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Semiconductor Microelectronics and Nanoelectronics Programs

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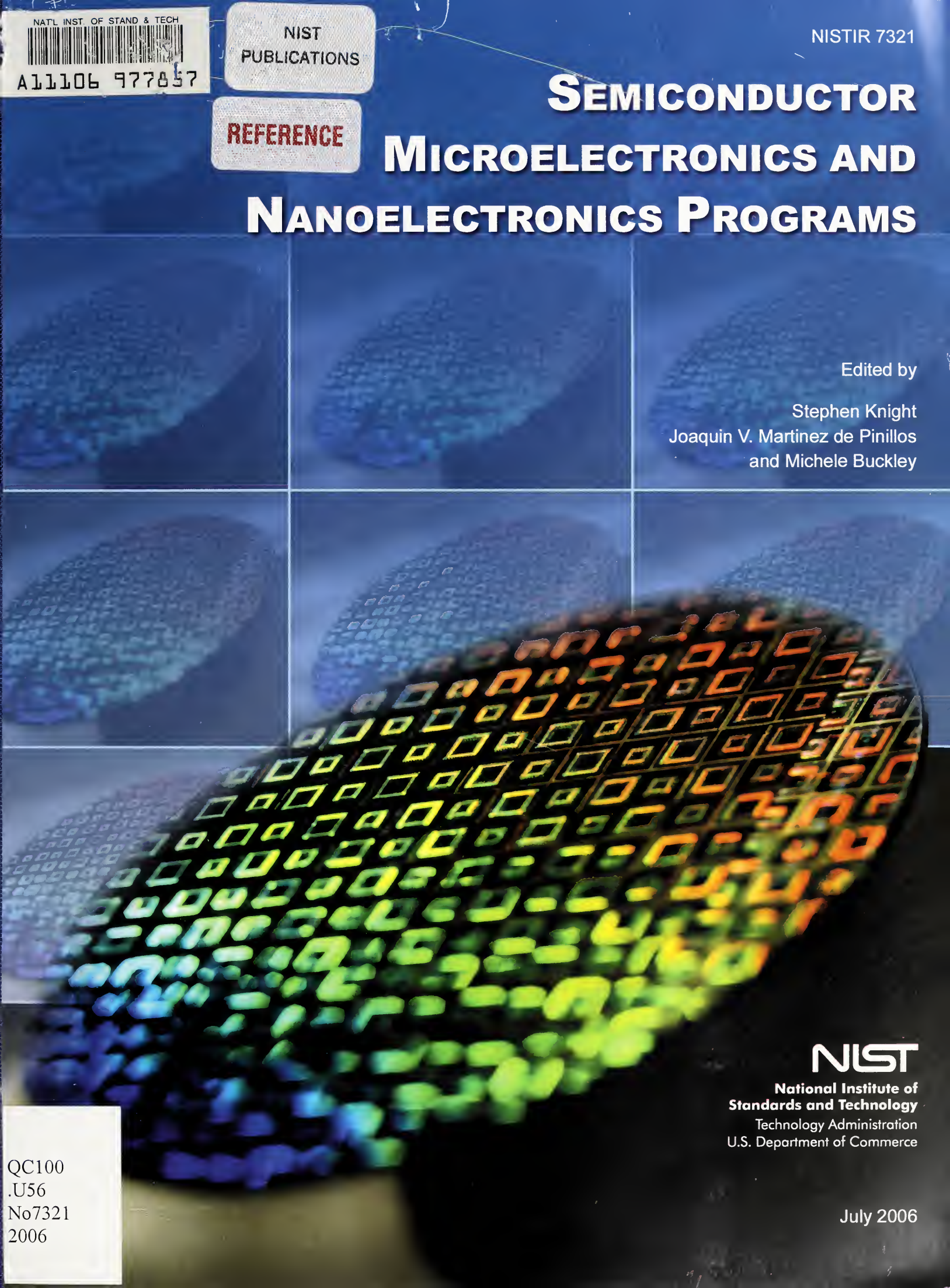

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Semiconductor Microelectronics and Nanoelectronics Programs

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July 2006

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References: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the most recent edition, dated 2005.

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2005 edition.* SEMATECH: Austin, TX, 2005.

This document is available on-line at URL: http://public.itrs.net or in printed copy by contacting SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, ITRS department 860-008, phone: (512) 356-3500.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

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Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the U.S. Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of 60 with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which is providing a $12 million budget in fiscal year 2006.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS), as well as on numerous SRC Technical Advisory Boards. NIST staff is also active in the semiconductor standards development work of the ASTM, the International National Electronics Manufacturers Initiative (iNEMI), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

Learn More About Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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From left to right: Joaquin Martinez de Pinillos, Stephen Knight, and Michele Buckley.

Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are in leading edge manufacturing facilities. The first 193 nm immersion lithography tools have been shipped to leading edge manufacturers and are being exercised for manufacture. High index fluids and lens materials for 193 nm tools are under intense exploration to develop high numerical aperture systems. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. At least three alpha tools will be shipped to development consortia in 2006. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials, and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.

Metrology Supporting Deep Ultraviolet Lithography

Goals

Develop solutions to key optical metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have created a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate optical measurements at DUV laser wavelengths.

A new lithography technology, immersion lithography, depends on incorporating a high-index fluid between the optical system and the wafer and possibly also incorporating a high-index material as the last lens element. Design and development of 193 nm and 157 nm immersion lithographies require accurate measurements of the index properties of the potential 193 nm and 157 nm fluids and materials.

To support these efforts, the National Institute of Standards and Technology (NIST), with SEMATECH, has developed a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential challenges for lithographic development are discussed in the 2005 International Technology Roadmap for Semiconductors. Page 1 of the Lithography section states: "Significant challenges exist in extending optical projection lithography at 193 nm wavelength using immersion lenses...." The need for advancing metrology in lithography is discussed on page 1 of the Metrology section: "Metrology continues to enable research, development, and manufacture of integrated circuits. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability."

Technical Strategy

- High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5 ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has begun constructing a new state-of-the-art minimum-deviation system and separately developed another system based on a vacuum ultraviolet (VUV) FT spectrometer and synchrotron radiation as a continuum source (see Fig. 1). Both of these systems will enable measurements to an accuracy of 1 ppm, and will be used to characterize high-index lens materials and immersion fluids for 193 nm and 157 nm lithography systems.

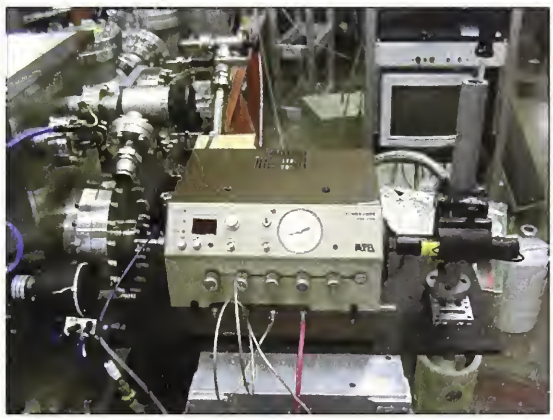

Figure 1. Facility for detector VUV radiation damage study using synchrotron radiation from SURF and a 157 nm excimer laser.

DELIVERABLES: Index measurement capability with 1 ppm uncertainty. 2Q 2006

Technical Contacts:
J. H. Burnett
M. Dowell

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild, Massachusetts Institute of Technology's Lincoln Laboratory

■ Taking full advantage of the potential resolution gain with immersion lithography may require using high-index materials as the last lens element, though as yet no such material has been demonstrated at 193 nm. To address this need we have begun, with the support of SEMATECH, a survey of candidate materials. We have identified several classes of oxide-based materials which have very high indices (near 2.0) at this wavelength and which can in principle be highly transparent at 193 nm. We have begun a program of complete optical characterization measurements of these materials to identify the most promising candidates and to assess their potential for development for lithography optics.

DELIVERABLES: Fully characterize the 193 nm optical properties of leading candidate high-index materials. 2Q 2006

■ An absolute light source in the DUV range based on synchrotron radiation using NIST's Synchrotron Ultraviolet Radiation Facility (SURF III) has been established using a dedicated beamline at SURF III. The flux of the DUV radiation at this beamline can be known to very high accuracy through the well established equations governing the behavior of the synchrotron radiation. The beamline is designed for customer calibration of a variety of DUV instruments to assist the development of the DUV lithography such as monochromators, discharge lamps, and irradiance meters. The spectral range covers all of the current important wavelengths for semiconductor industry such at 248 nm, 193 nm, 157 nm and even down to 13 nm. The uncertainty of such calibration is better than 1 % in the case of deuterium lamp calibration.

DELIVERABLES: Provide customer DUV calibration for discharge lamps, monochromators, and irradiance meters using SURF III source-based beamline with highest accuracy. Ongoing

■ Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, and specifically KrF (248 nm) and ArF (193 nm), excimer lasers, are the preferred sources for high-resolution lithography at this time. In addition, we can provide calibrations for F_2 (157 nm) excimer lasers. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 nm and 248 nm, and 157 nm. Figure 2 shows the excimer laser calibration facility.

Figure 2. Laboratory for excimer laser energy and power meter calibrations, with measurement systems for 248 nm, 193 nm, and 157 nm. The excimer lasers are along the top right and the enclosures for nitrogen gas purging are in the foreground.

DELIVERABLES: Proven high-quality calibration services, and supporting measurements for excimer laser power and energy meters to the Semiconductor Industry at 248 nm, 193 nm, and 157 nm. Ongoing

Accomplishments

■ We have used our Hilger-Chance refractometer system to assist the industry in the search for appropriate high-index fluids (with n greater than water, 1.4366 at 193 nm) for possible use in immersion photolithography. In addition to providing measurement services to several companies which are developing new fluids for 157 nm and 193 nm lithography, we have performed our own survey of fluids at 193 nm. The results are shown in Fig. 3. As this figure shows, there are a number of fluids which are transparent at 193 nm and have n larger than water, up to 1.62 for glycerol. However, the thermo-optic coefficient, dn/dT, is larger as well, which may make the use of these difficult in a commercial stepper system because of thermal stability issues.

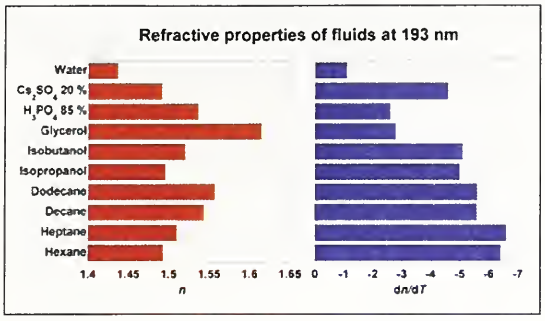

Figure 3. Measured index of refraction n and thermo coefficient dn/dT of a number of potential immersion fluids for 193 nm lithography.

■ We have performed additional measurements of the effect of dissolved air on the refractive index of water at several wavelengths in the visible and UV and compared the results with predictions based on the equation of state of water and the known partial molar volumes and polarizabilities of the soluble components of air. The data and model calculations are in reasonable agreement, and demonstrate that the magnitude of the effect gets larger at shorter wavelength, up to -6.7×10^{-6} at 193 nm. While industry uses degassed water for immersion lithography, our results will enable any potential optical distortions due to air exposure to be modeled at the system level.

■ We have identified four major classes of oxide-based materials that have potential to be used as high-index lens materials for enabling further feature-size reduction with immersion lithography. The four classes are: (1) Group II oxides, *e.g.*, MgO, (2) crystalline spinel ($MgAl_2O_4$) and its variants, (3) a ceramic form of spinel, and (4) aluminum garnets, *e.g.*, YAG. We have made preliminary characterization measurements of the key 193 nm optical properties (see Fig. 4), including the intrinsic birefringence, of members of each of these classes needed to assess their suitability. As a result of these measurements, several potentially feasible candidates have been established.

■ We have constructed a radiometric facility tailored for the DUV range using a beamline at NIST's SURF III with the radiation measurement scale derived from a high-accuracy cryogenic radiometer. The beamline is designed for very general-propose high-accuracy measurements. We have used this facility to measure DUV general material properties such as transmission and reflectance. Examples of such measurements include DUV mirrors, windows, filters, and also the transmission and absorption of liquids that could be used for immersion lithography. On the detector side, we have calibrated and characterized a variety of DUV detectors such as solid state photodetectors, solar-blind detectors, photoconductive detectors, and pyroelectric detectors. We also performed irradiance calibrations for DUV irradiance meters.

■ We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation (see Fig. 5) and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen

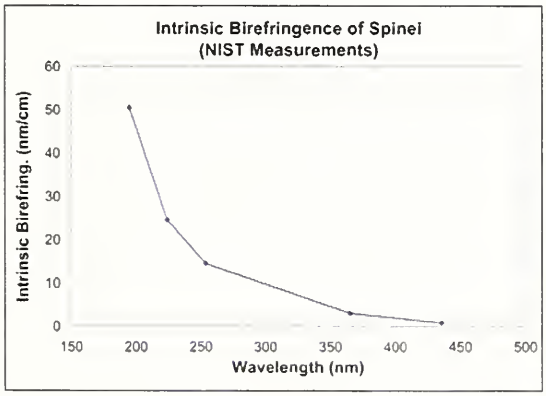

Figure 4. Measured intrinsic birefringence of crystalline spinel vs. wavelength.

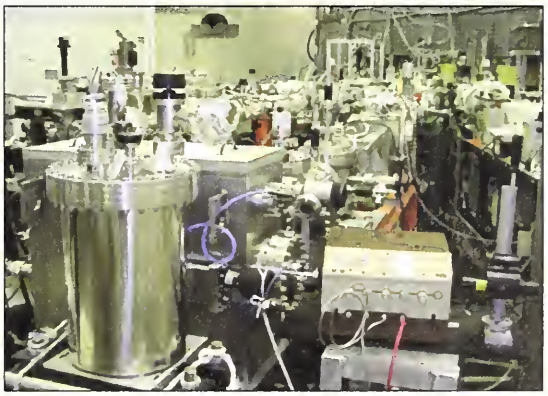

Figure 5. Measurement system for detector damage study by a 157 nm pulsed excimer laser.

in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes. For example, we have determined that for silicon photodiodes under irradiation with a 157 nm excimer laser, an important mechanism for the degradation is the formation of trap states at the interface of the silicon-silicon dioxide induced by the damaging radiation. These trap states act as recombination centers and reduce the yield of electric current generated by incident radiation. A model was developed to simulate the change in response for photodiode irradiated by 157 nm radiation.

■ During the last 15 years we have developed a suite of laser calorimeter standards for 248 nm, 193 nm, and 157 nm excimer laser energy and power measurements traceable to SI units. The 248 nm and 193 nm calorimeters use a specially designed absorbing cavity with a volume absorbing glass to reduce potential damage to the cavity by the high peak power in the UV laser pulses. The 157 nm calorimeter is a fundamentally new type of laser calorimeter standard that uses a thin-walled SiC absorbing cavity, which is designed to completely absorb and spread the incoming laser energy through multiple reflections. All of these calorimeters are calibrated using an imbedded electrical heater that allows for traceability to SI units through electrical standards of resistance and voltage. Calibrations for industry customers are accomplished for each wavelength with appropriate measurement systems that involve purging of oxygen to eliminate atmospheric absorption of the laser radiation.

■ As a further extension of our excimer laser services we have developed the capability to directly measure UV irradiance or "dose" at 248 nm and 193 nm, which involves homogenizing the beam profile and measuring the energy transmitted through a calibrated aperture. This capability can improve accuracy for customers who need to measure the energy absorbed at a surface such as at the wafer plane.

■ We have also developed the capability to characterize the nonlinear response of 193 nm and 248 nm excimer laser detectors based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. Using this system, one can easily determine problems such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise (see Fig. 6).

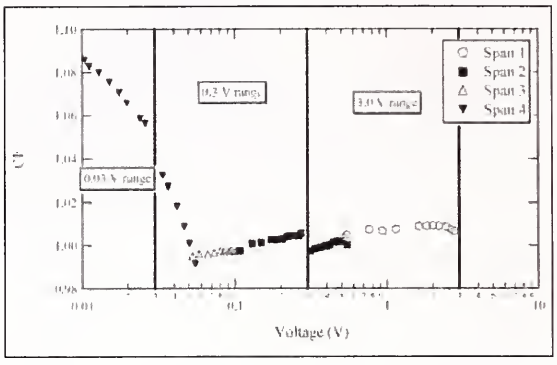

Figure 6. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

■ We completed the first internal comparison of the NIST UV excimer laser calorimeters. This work includes measurements taken over the course of a two-year period in which the performance of the NIST 157, 193, and 248 nm excimer laser calorimeters was monitored at the design wavelengths as well as at the other excimer laser wavelengths. The results show good agreement among the transfer standards and excellent stability over time. From these data, we determined that the responsivity of the NIST UV laser calorimeters all agree within their stated uncertainties. In all but one case, the calorimeters' responsivities agree to better than 0.3 %. The comparison between the DUV (193 nm) and UV (248 nm) calorimeters at 248 nm uncovered a 1 percent difference between the calorimeters' responsivities. This difference is due to partial transmission of the 248 nm radiation through the absorbing glass of the DUV calorimeter which, reduces the calorimeter's absorptance and alters its response.

Collaborations

Air Products and Chemicals, Inc., Bridgette Budhlall, immersion photolithography fluid development.

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Metrology Supporting Extreme Ultraviolet Lithography

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C. Tarrio
S. Grantham
U. Griesmann
S. Hill

Goals

Provide leading-edge metrology for the development and characterization of sources, optical components, and dosimeters used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

An intense international effort is presently underway to install EUVL into commercial production in 2011 at the 32 nm node. As part of that effort, ASML will deliver two alpha-generation steppers for initial testing later this year.

Several significant challenges to commercialization of EUVL remain, including source power, optics lifetime, and optics and mask fabrication. The associated metrological challenges include the development of: (1) highly precise extreme ultraviolet (EUV) reflectometry; (2) accurate pulsed EUV radiometry for source comparisons and wafer-plane dosimetry; (3) accelerated testing techniques for optics lifetime characterization; and (4) nanometer-level optical figure measurement.

Technical Strategy

1. Precise EUV Reflectometry

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics up to 40 cm in diameter and 40 kg in mass. The facility has a demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.001 nm, with plans under-way to improve each accuracy by a factor of two in the near future.

Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has also been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements in support of EUVL performed recently are the radiometric calibration of the "Flying Circus II" and "E-Mon" radiometers used for the comparison of source outputs, resist dosimetry, and determination of EUV optical constants through angle dependent reflectance measurements. The reflectivity of a typical mirror designed for use in a EUVL stepper is shown in Fig. 1.

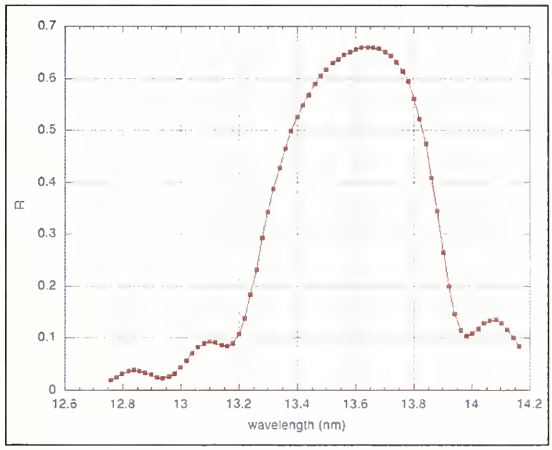

Figure 1. Reflectivity vs. wavelength of a typical MoSi multilayer mirror. The measurement was made at 5° from normal incidence.

DELIVERABLES: Full reflectivity maps of EUV mirrors up to 40 cm in diameter and 45 kg in mass on an as needed basis for the EUVL community. Many other types of EUV measurements including transmission, resist dosimetry and other testing, and cw radiometric calibrations of fully assembled filter radiometers used in source comparisons.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. The Photon Physics Group is responsible for maintaining the spectral responsivity standards in the far- and extreme-ultraviolet spectral regions, including 13.5 nm, the EUVL wavelength of interest. We operate several beamlines at the SURF III synchrotron radiation facility, a quasi-cw source, as well as laser-produced plasma source, which is pulsed with a 10 ns pulse length. With these facilities, we can calibrate EUV detectors and dosimeter packages under either cw or pulsed conditions.

A major concern when using solid state photodiodes for detection of short pulse length radiation is that the detector may saturate under the high peak power, even though the average power is moderate. We have measured the saturation characteristics of EUV sensitive Si photodiodes using 532 nm radiation as a proxy for 13.5 nm; the

absorption characteristics in Si are nearly identical. This proxy procedure has been validated by correcting a 13.5 nm pulsed calibration for saturation in both the sample radiometer and the standard photodiode using saturation data obtained at 532 nm. The corrected results were in good agreement with individual component calibrations, while the uncorrected results were not.

We have found that the photodiode responsivity is an inherently non-linear function of pulse energy, but the responsivity can be fit by a calibration function having two constant parameters. Use of the non-linear calibration function allows the photodiode to be used with reasonable uncertainty even when the responsivity has decreased due to saturation effects by as much as a factor of two. We have developed a model of the physical processes that are responsible for saturation. The loss of total collected charge is modeled as a result of recombination processes in the device during the electronic readout time. The model correctly predicts the behavior of both calibration parameters as a function of reverse bias in the range from 0 V to 150 V and spot sizes greater than 0.01 mm^2. We have found no dependence on pulse length from 10 ns to 1 μs, indicating that the effects of saturation are the same for laser-produced plasma sources and for the pinched plasma sources with longer pulse lengths. There is substantial deviation from the expected saturation behavior as the illuminated area decreases (*i.e.*, the energy density increases) to very small spots sizes (less than 0.01 mm^2). The measured saturation loss is less than our model predicts, probably due to lateral diffusion current that decreases the local carrier density. It has been reported previously that the low-power limit of the pulsed responsivity is equal to the responsivity measured with a low-power, cw source. Combining these results, it is possible to transfer a continuous wave (cw) calibration to a pulsed application with low uncertainty.

In 2006, we will participate in an international intercomparison of EUV detector responsivity. This intercomparison will establish the worldwide equivalence of detector responsivity measurements from the major National Metrology Institutes performing these calibrations. We will also work to expand our EUV measurement capabilities to include measurements of EUV spectrograph and CCD responsivity to further aid the EUV lithography community.

DELIVERABLES:

- EUV detector responsivity international intercomparison. 3Q 2006
- EUV CCD responsivity measurement. 3Q 2006
- EUV spectrograph measurement. 4Q 2006

3. EUV Damage Characterization

One of the potential showstoppers for commercialization of extreme ultraviolet lithography (EUVL) is the degradation of the multilayer-mirror stepper optics. The mirrors lose reflectivity because adsorbed contaminant gases such as hydrocarbons and water are cracked by the energetic (13.5 nm) photons. This leads to growth of an amorphous carbon layer on the optics surfaces or to oxidation of the optics themselves. The former effect is largely reversible; however, the latter is not. Unfortunately, these ambient contaminants cannot be eliminated by baking because the alignment of the mirror stack must be maintained to submicron tolerances. Various capping layers are currently being developed to extend the lifetime of the multilayer mirrors towards the required goal for commercialization of only a few per-cent reflectivity loss over 30000 hours (h) of use.

To study the effectiveness of new capping layers and to better understand the underlying processes responsible for mirror degradation, NIST has commissioned a new beamline at the Synchrotron Ultraviolet Radiation Facility (SURF III) that can expose capped-multilayer samples to ≈ 6 mW/mm^2 of 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures up to 6.7×10^{-4} Pa. To date the most successful capping layer available to the community has been ~ 2 nm of ruthenium. Our exposure facility has demonstrated that multilayers with this capping layer suffer approximately one-tenth the reflectivity loss of bare Si-capped multilayers when exposed for $\approx$ 100 h under rather aggressive conditions of 1×10^{-4} Pa of water vapor.

Clearly, testing multiple capping layers for the required 30000 h optic-lifetime is not feasible. We have therefore developed a program for accelerated lifetime testing in which multilayers are exposed to various EUV intensities under various high-vacuum environments. The ultimate goal of this program is to develop a model of mirror damage that will enable the extrapolation of the years-long-lifetime under normal operating conditions from a few hundred hours of exposure under appropriately chosen accelerated exposure conditions. This effort requires an understanding of the

underlying damage mechanisms that are being studied by an iterative series of controlled exposures and analysis. In addition to measuring the reflectivity loss of exposed multilayers (Figure 2), the damage will be characterized using a range of surface analysis techniques. Although this effort is just beginning, we have already discovered that small levels of hydrocarbons (1×10^{-7} Pa) can completely determine the rate of mirror damage, even in the presence of much larger partial pressures of water vapor (7×10^{-4} Pa). Thus, the vacuum environment must be carefully controlled and well characterized for any accelerated testing procedure to produce meaningful results.

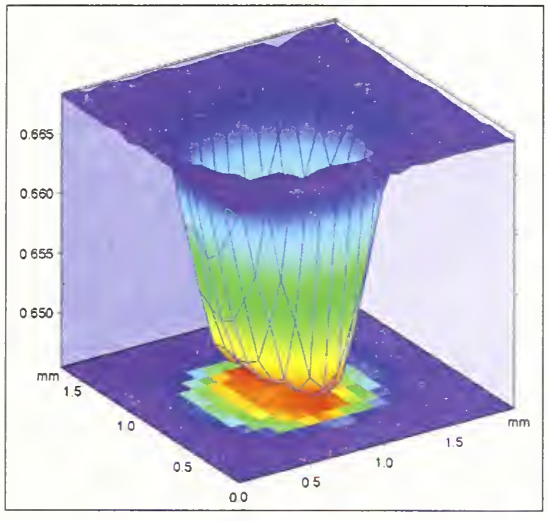

Figure 2. Spatial mapping of the reflectivity of a multilayer mirror following exposure to EUV under aggressive environmental conditions.

To respond to the growing need for optic-lifetime characterization we have continued to expand our capabilities. The original lifetime testing chamber was developed with support from Sematech and Sandia National Labs. Recently, a second beamline with a lifetime testing chamber has been constructed and commissioned with industry support. In addition, with intramural support from the NIST Advanced Technologies Program, we are installing a pulsed source so that mirror degradation caused by the quasi cw irradiation of the SURF synchrotron can be compared with that caused by pulsed irradiation. In addition to expanding our facilities, we have also established very fruitful collaborations with experts in surface science both within and outside the NIST community.

DELIVERABLES:

- Commission new lifetime testing beamline. 2Q 2006
- Work with industrial collaborators to evaluate titanium dioxide as a possible capping layer. 4Q 2006
- Install pulsed EUV source for testing under pulsed irradiation. 4Q 2006

4. Sub-nm Uncertainty Optical Figure Measurement

The commissioning of the "eXtremely accurate CALIBration InterferometeR" (XCALIBIR) at NIST is now complete and the instrument is fully functional (Fig. 3). The XCALIBIR interferometer is a multi-configuration precision phase-measuring interferometer for optical figure measurements of flat, spherical and aspheric optics that can achieve the very low measurement uncertainties that are required for the measurement of EUVL optics.

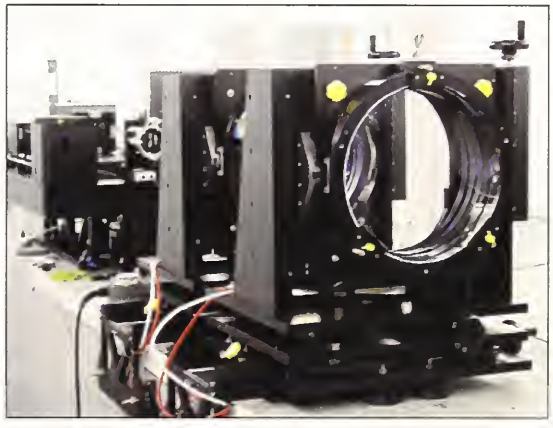

Figure 3. A view of the XCALIBIR interferometer.

The XCALIBIR interferometer may be operated in either Twyman-Green or Fizeau configurations. A beam expander in the test arm of the interferometer provides a collimated test beam with 300 mm diameter. Transmission spheres are used to realize a spherical Fizeau interferometer for the testing of spherical and aspheric surfaces. The part under test is mounted on a remotely controlled 5+1-axis mount that can be moved on air bearings along a precision slideway in the direction of the optical axis of the interferometer. A system of three laser-interferometers tracks the movement of the test mount in the direction of the optical axis. A single-mode external cavity diode laser (ECDL) is used as the light source in XCALIBIR. The laser frequency can be modulated to vary the effective temporal coherence over a wide range. Optical fibers with different core diameters are used to couple the light into the interferometer. The spatial coherence of the light source can thus be varied by using fibers with different core diameter.

The 300 mm diameter reference flats for the flat Fizeau configuration of the interferometer were calibrated with a 3-flat, 6-position self-calibration test. Figure 4 shows the topography of one of the reference flats. A large number of 3-flat measurements were made to estimate the measurement uncertainty. For each of the flats A, B, and C the *rms* of the difference between the averaged flat solutions and the individual measurements was plotted in a histogram (Fig. 5). A (statistical) measurement uncertainty of approximately 0.2 nm rms is evident.

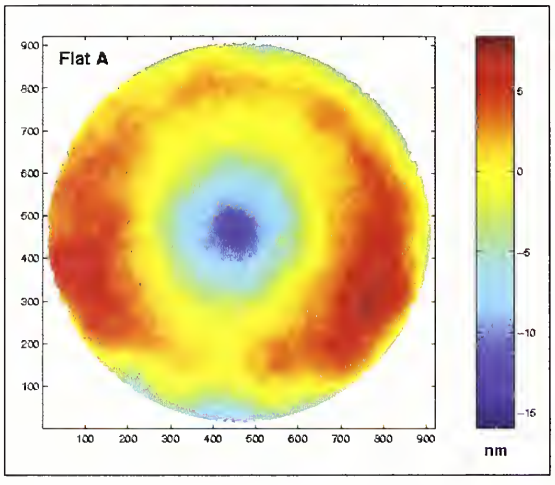

Figure 4. Topography of a 300 mm diameter XCALIBIR reference flat.

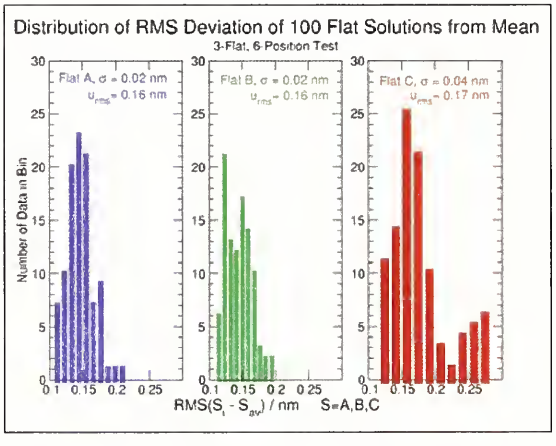
Distribution of RMS Deviation of 100 Flat Solutions from Mean
3-Flat, 6-Position Test
Flat A, σ = 0.02 nm
Flat B, σ = 0.02 nm
Flat C, σ = 0.04 nm
Number of Data in Bin
RMS(S_i - S_av) / nm S=A,B,C

Figure 5. Distribution of rms *deviations from best estimates surface (mean) for three flats A, B, and C.*

When measurements of aspheric optics without null-optics are made, it is frequently the case that only a part, or subaperture, of a surface can be measured at once. For the figure measurement of the entire aspheric surface a number of overlapping subaperture measurements must then be combined, or "stitched" together. We have implemented flexible and robust algorithms for the stitching of subaperture measurements. To demonstrate the power of the stitching algorithm a precision silicon sphere with 96.4 mm diameter (a 1 kg mass sphere) was set up on a rotary table in XCALIBIR and the surface figure error was measured with an F/1.3 transmission sphere. 138 surface error measurements were made at 10° intervals. As shown in Fig. 6, the individual, overlapping, surface error measurements were then stitched together to form a map of the form error of the silicon sphere.

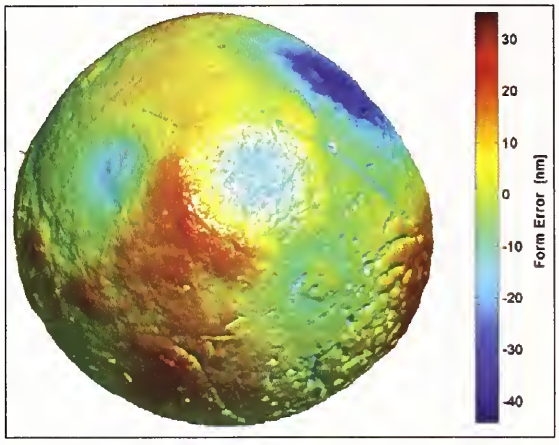

Figure 6. Deviation from perfect spherical form of a 1 kg precision silicon sphere.

In addition to the XCALIBIR interferometer, we are developing a new metrology tool for the measurement of aspheric and free-form precision surfaces, the Geometry Measuring Machine (GEMM). In its current form, GEMM is a profilometer for free-form surfaces. A profile is reconstructed from the local curvature of a test part surface, measured at several locations along a line. For profile measurements of free-form surfaces, methods based on local part curvature sensing have strong appeal. Unlike full-aperture interferometry they do not require customized null optics. The uncertainty of a reconstructed profile is critically dependent upon the uncertainty of the curvature measurement and, to a lesser extent, on curvature sensor positioning accuracy. The new instrument, shown in Fig. 7, provides an alternative means for validating the measurements made with XCALIBIR.

DELIVERABLES: Validation of stitching method for form error measurements of aspheric surfaces with low uncertainty. This will be done with an industrial collaborator. 4Q 2006

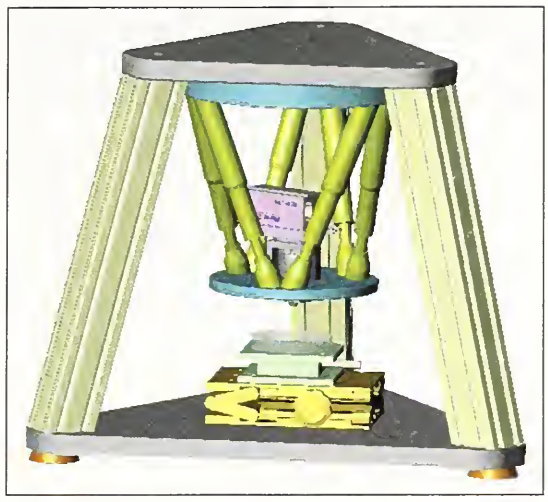

Figure 7. Geometry Measuring Machine (GEMM) for form measurements of free-form precision surfaces.

Collaborations

VNL at Lawrence Livermore National Laboratory, Saša Bajt, EUV Multilayer Development and Coating Team.

Recent Publications

S. Grantham, C. Tarrio, R. E. Vest, and T. B. Lucatorto, *"Metrology for EUVL Sources and Tools, in EUV Sources for Lithography,"* V. Bakshi, ed. (SPIE Press, Bellingham, WA, 2006).

R. E. Vest, Y. Barad, M. L. Furst, S. Grantham, C. Tarrio, and P. S. Shaw, *"NIST VUV Metrology Programs to Support Space-Based Research,"* Advances in Space Research **37**, 283-296 (2006).

R. E. Vest, S. Hill, and S. Grantham, *"Saturation effects in solid-state photodiodes and impact on EUVL pulse energy measurements,"* Metrologia **43**, S84-S88 (2006).

S. M. Owens, J. S. Gum, C. Tarrio, S. Grantham, J. Dvorak, B. Kjornrattanawanich, R. Keski-Kuha, R. J. Thomas, C. C. Kankelborg, *"Narrow-band EUV multilayer coating for the MOSES sounding rocket,"* in Proc. SPIE Vol. 5900, Optics for EUV, X-Ray, and Gamma-Ray Astronomy II, pp. 5-13 (2006).

U. Griesmann, *"Three-Flat Test Solutions Based on Simple Mirror Symmetry,"* Appl. Opt. 2006 (in press).

N. Machkour-Deshayes, J. Soons, U. Griesmann, R. S. Polvani, J. Stoup, and Z. Q. Lu, *"Form-profiling of optics using the Geometry Measuring Machine and the M-48 CMM at NIST,"* Accepted for publication in J. Res. NIST (2006).

S. Grantham, C. Tarrio, S. B. Hill, and T. B. Lucatorto, *"Optics go to extremes in EUV Lithography,"* Laser Focus World, Vol. **41**, no. 11, pp. 117-122 (2005).

C. Tarrio and S. Grantham, *"A synchrotron beamline for extreme-ultraviolet multilayer mirror endurance testing,"* Rev. Sci. Instrum. **76**, 056101 (2005).

C. Tarrio, S. Grantham, R. E. Vest, and K. Liu. *"A simple transfer-optics system for an extreme-ultraviolet synchrotron beamline,"* Rev. Sci. Instrum. **76**, 046105 (2005).

U. Griesmann, N. Machcour-Deshayes, J. Soons, B. C. Kim, Q. Wang, J. R. Stoup, and L. Assoufid, *"Uncertainties in aspheric profile measurements with the Geometry Measuring Machine at NIST,"* in Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies II; Angela Duparre, Bhanwar Singh, Zu-Han Gu; Eds., Proc. SPIE **5878**, 112-124 (2005).

U. Griesmann, Q. Wang, J. Soons, and R. Carakos, *"A simple ball averager for reference sphere calibrations,"* Optical Manufacturing and Testing VI; H. Philip Stahl; Ed., Proc. SPIE **5869**, 189-196 (2005).

U. Griesmann, J. Soons, and Q. Wang, *"Measuring Form and Radius of Spheres with Interferometry,"* Annals of the CIRP **53**, 451-454 (2004).

W. M. Clift, L. E. Klebanoff, C. Tarrio, S. Grantham, O. R. Wood II, and N.V. Edwards, *"Scaling studies of capping layer oxidation by water exposure with EUV radiation and electrons,"* SPIE vol. 5374, Emerging Lithographic Technologies VIII p. 666 (2004).

Polymer Photoresist Fundamentals for Next-Generation Lithography

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E. K. Lin
W. L. Wu

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The understanding developed in this program will provide a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 50 nm structures. The unique measurement methods we apply include X-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), nuclear magnetic resonance (NMR), atomic force microscopy (AFM), fluorescence correlation spectroscopy (FCS) and combinatorial methods. Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the physical properties of and polymer chain conformation within sub 50 nm structures; (2) the spatial segregation and distribution of photoresist components; (3) the transport and kinetics of photoresist components, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermo-physical properties of interfaces as applicable to immersion lithography. These data are needed to meet the future lithographic requirements of sub 50 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility for development in an aqueous base solution. These reaction-diffusion, and development processes must be understood and controlled at the nanometer length scale to fabricate effectively integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 50 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 50 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm or EUV) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, component distribution, or transport properties. Furthermore, the required resolution for a sub 50 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2005 International Technology Roadmaps for Semiconductors on page 9, Lithography Section, "Photoresists need to be developed that provide good pattern fidelity, good line width control, low line width roughness, and few defects. As feature sizes get smaller, defects and monomers will have comparable dimensions with implications for the filtering of resists."

"[This work] opens a window of opportunity to construct structure-property relationships between chemical transport mechanisms and ultimate resist resolution. It may also lead to insights into the ultimate, intrinsic resolution limits and critical dimension control of polymer-based imaging materials."

E. Reichmanis and O. Nalamasu, Bell Labs, Lucent Technologies, Science, 297, 349 (2002).

Technical Strategy

In this project, we use model photoresist materials to validate the new measurement methods. Model photoresist materials (248 nm, 193 nm, 157 nm, and EUV) have been used initially to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the deprotection reaction kinetics, and the physics of the development process. We also are adapting the application of combinatorial methods as a tool to determine rapidly important lithographic parameters and to identify material factors impacting feature resolution. These results provide a basis for understanding the material property changes that may affect the development of lithography for sub-50 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance.

DELIVERABLES:

- Develop model thin films to measure the transport and kinetics of photoresist components and the deprotection reaction as a function of PAG size and resist copolymer chemistry. 2Q 2006
- Conclude protection degree effect on the dissolution and swelling behavior and the relationship to surface roughness for 193 nm photoresist polymers. 2Q 2006
- Utilize reaction-front bilayer geometry to identify and quantify the effects of developer solution parameters (base concentration, ionic strength) on the final resolution of lithographic materials. 3Q 2006
- Quantify surface segregation, surface deprotection chemistry, distribution of photoresist components (resist, photoacid, base additive) in 193 nm resists, using NEXAFS. 4Q 2006
- Conclude PAG loading effect on the dissolution and swelling behavior and the relationship to surface roughness for model EUV photoresist polymers. 4Q 2006
- Quantify the effect of dose on the form and spatial extent of photoacid diffusion at model lithographic line edges for EUV photoresist. 2Q 2006

Accomplishments

■ The molecular origin of dimensional changes within ultrathin films when exposed to developer solutions was measured using neutron reflectivity. A model photoresist material provided needed in the fundamentals of material sources to line-edge roughness. Quartz crystal microbalance measurements complement these measurements with the added ability to measure the kinetics of swelling, however, the profile and chemical specificity are exclusively obtained with NR.

These new measurement methods, applicable to immersion lithography, demonstrate that swelling and aqueous base penetration must be considered to improve dissolution models involving solid-liquid interfaces. The aqueous base profile, shown in Fig. 1, illustrates the penetration of the small base molecule throughout the thin film as a function of developer strength. The swelling, due to polyelectrolyte effects, was predicted in FY03. The influence of moisture and interfacial energy are also probed using NR, XR, and quartz crystal microbalance techniques, allowing complete equilibrium and kinetics measurement methods.

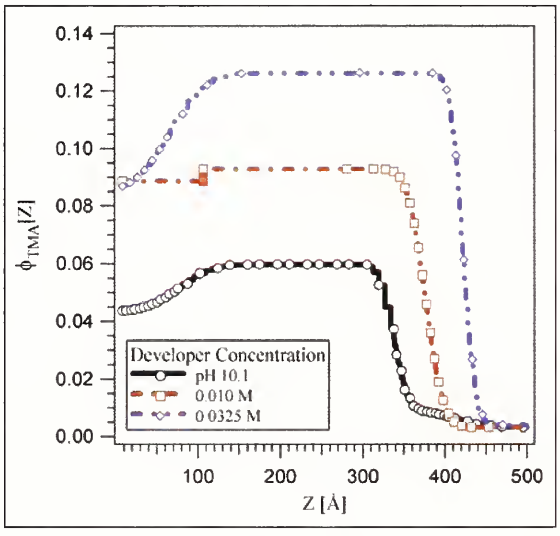
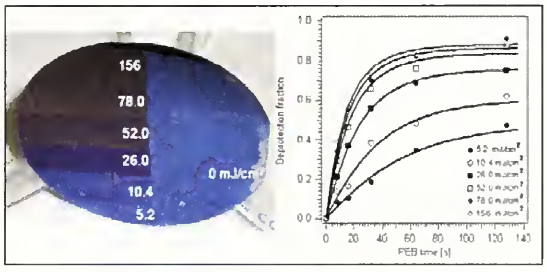


Figure 1. Developer Fundamentals for LER. Direct measure of the base concentration dependence of swelling and deuterated tetramethyl ammonium ion profile throughout the thickness, of a model 157 nm photoresist using liquid immersion neutron reflectivity.

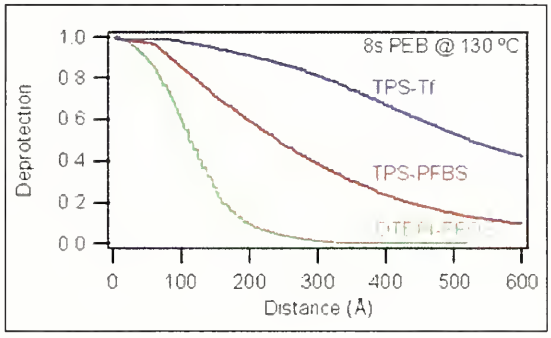
■ The kinetics of an acid-catalyzed deprotection reaction in model photoresist materials was studied as a function of copolymer composition with Fourier transform infrared (FTIR) spectroscopy. Three methacrylate-based terpolymers with varying compositions of acid-labile and non-reactive (lactone) monomers were studied. A mathematical model was developed to analyze the acid catalyzed deprotection kinetics with respect to coupled reaction rate and acid-diffusion

processes. The first order reaction rate constant decreases as a non-reactive comonomer content is increased. Additionally, the extent of reaction appears self-limiting as verified by a slowing down necessitating an acid-trapping chemical equation to model the data. An example is shown in Fig. 2. This composition-dependent reaction constant indicates a strong interaction of the acid with the increasing polar resist matrix that drastically reduces the acid transport rate. The severely reduced acid transport is consistent with hydrogen bonding between photoacid and methacrylic acid product. These results demonstrate a correlation between polymer microstructure and acid catalyzed kinetics; necessary measurements for analysis of coupled reaction-diffusion processes. Finally, the models were applied to understand the limiting spatial extent of photoacid diffusion at the model line edge determined by neutron reflectivity.



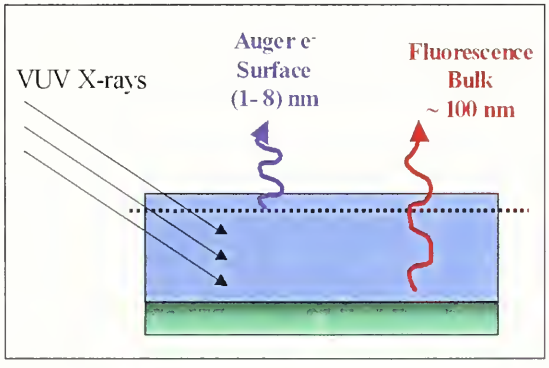
Fignre 2. Wafer after exposnre to varied DUV dose and fixed baking time the color change represents slight changes in film thickness with extent of reaction. Qnantification of the extent of reaction (deprotection fraction) versns post-exposnre bake time for model 193 nm resist for varying dose.

■ The deprotection reaction front profile was measured with nanometer resolution by combining neutron reflectivity and FTIR on a bilayer structure prepared with model 193 nm photoresists. The upper layer of the structure is loaded with the photoacid generator. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group partially leaves the film, quantified by FTIR, upon reaction. The contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that the reaction front width is dependent upon resist chemistry and PAG size as shown in Fig. 3. These experimental data provide a rational design of next-generation photoresist component from the resist chemistry to the reaction-diffusion process.



Fignre 3. Nentron reflectivity resnlts of the nanometer scale deprotection profile shape dependence on photoacid generator size: TPS-Tf < TPS-PFBS < DTBPI-PFOS. These high-resolntion experimental data help verify current advanced reaction-diffusion models.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment in Fig. 4. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined.



Fignre 4. Schematic diagram of the NEXAFS measnrement geometry. Spectra are obtained from the film snrface and bulk simnltaneously.

Different chemistries may be observed by examining the near-edge X-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer chemistry and PAG size. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stability against model airborne contaminants and influence on *in-situ* processing.

- NEXAFS measurements were used to measure the surface concentration and depth profile of photoacid generators for advanced 193 nm photoresist materials for immersion lithography. These measurements quantify the influence of water immersion on the loss of these critical components. NEXAFS on wafer analysis combined with LC/MS demonstrate that equilibrium water solubility of PAGs with varying perfluoroalkyl length does not serve as the appropriate criteria for selecting PAGs for immersion lithography; rather the segregation of PAGs to the top few nanometers provides the majority of leaching as shown in Fig. 5. Additionally, the effects of critical top coats are also investigated to understand the segregation and retention of PAG additives.

- The development step selectively removes UV exposed photoresist material and represents the last step in the fabrication of nanostructures prior to semiconductor etch and deposition. With dimensions shrinking to sub-50 nm, control of line-edge roughness becomes more important and contributions to roughness from the development step requires an improved framework. In the development step, the aqueous base TMAH developer shifts the local chemical equilibrium from an unionized form to the ionized form, for instance in the 248 nm material poly(hydroxystyrene). SANS data, in Fig. 6, demonstrate the origin of the miscibility in aqueous base is due to the ionization of the photoresist leading to polyelectrolyte behavior. The identification of the presence of polyelectrolyte behavior during the development process provides an improved framework to understand the roles of added electrolytes, such as low molecular weight organic (tetramethylammonium chloride) and inorganic salts (NaCl, KCl). The addition of salts reduce the influence of polyelectrolyte behavior. Current experiments with different developing and rinsing protocols demonstrate that the pH of the rinse step is very important. This suggests the surface layer may contain polyelectrolyte effects even after development as demonstrated by an increase in surface RMS roughness for the development of bilayer samples with 0.26N TMAH followed by water rinse and 0.01 M HCl rinse.

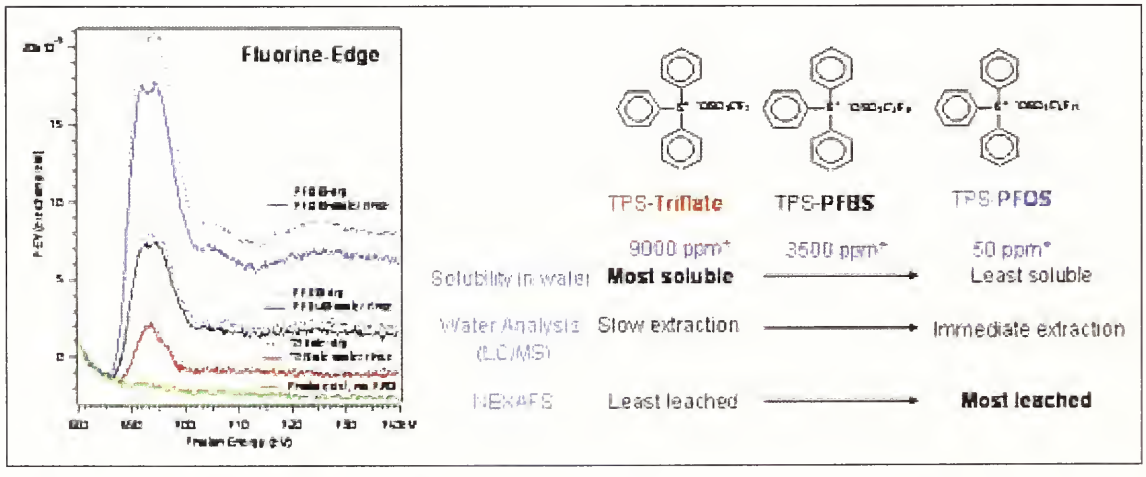


Figure 5. NEXAFS fluorine-edge experimental results quantifying the extent of PAG loss from the surface due to water immersion. The series of PAGs tested for immersion lithography is shown as a function of equilibrium water solubility, extraction from thin films, and NEXAFS surface composition analysis.

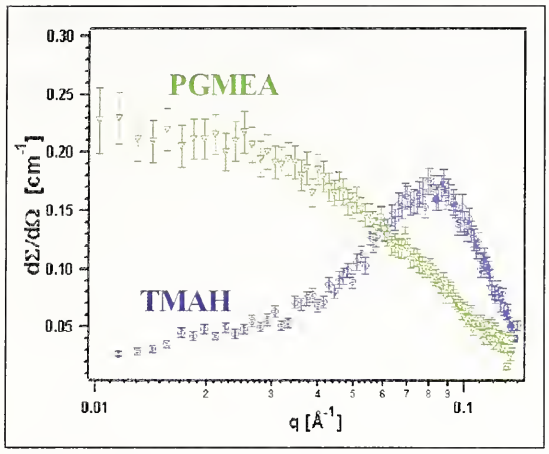


Figure 6. SANS data from a model photoresist polymer in organic solvent (PGMEA) and the developer base solution (TMAH). The scattering peak in TMAH solution is representative of the polyelectrolyte behavior.

■ Characterization of local bulk scale mixing is neeessary for understanding future photoresist materials as feature dimensions are reduced to sub-65 nm. The intimacy of mixing of PAG and photoresist was probed by solid state proton NMR methods based on inversion-recovery, solid-eeho-spin-diffusion, and chemical-shift-based-spin-diffusion pulse sequences. The effect of PAG concentration on the dispersion and phase separation within bulk blends was found to depend strongly on the photoresist chemistry (see Fig. 7). In model 248 nm materials PFOS was found to mix on the molecular scale for loadings between 9 % and 45 %; hence the two components are thermodynamically miscible in this range.

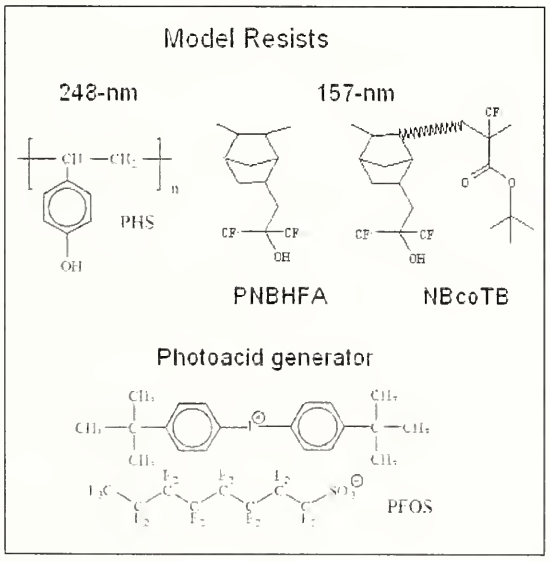


Figure 7. Model 248 nm and 157 nm photoresist materials used to probe the intimacy of mixing of photoacid generator in blends by NMR methods.

These results were extended to a challenging 157 nm formulation and revealed that, while PFOS is miscible within the two photoresists, the ternary system exhibits phase separation into domains exceeding 30 nm.

■ EUV photoresist polymers are expected for imaging at the 32 nm node and smaller. Similar to 193 nm the deprotection reaction front profile is a critical factor. However, in particular to EUV photoresists high PAG loading as well as lower EUV doses are expected. We applied neutron reflectivity to understand the effect of dose using model deuterated polymeric resists as shown in Fig. 8. The deprotection fronts exhibits two different length scales; a slow front that initiates high degrees of deprotection near the interface and a fast front that propagates into the resist with reaction-diffusion lengths consistent with those reported in the literature. However, the deprotection level and diffusion-length scale are exposure dose (photoacid coneentration) dependent. The origin of the fast-diffusion front dependence on dose was hypothesized due to the increase in copolymer composition polarity as the reaction proceeds thereby limiting the spatial-extent. The evolving copolymer composition appears central in future modeling of latent image profiles. Neutron reflectivity was demonstrated to have sufficient chemical sensitivity and spatial resolution to measure the interfacial structure on sub-nm length scales. This approach can be extended to understand the effects of additives, such as photodegradable bases, as well as different architecture such as the molecular glass photoresists shown in Fig. 8. The effect of architecture or "pixel size" may also play a crucial role to higher fidelity imaging. We develop dissolution fundamentals to help quantify the effects of swelling and dissolution rate on the effect of resist architecture.

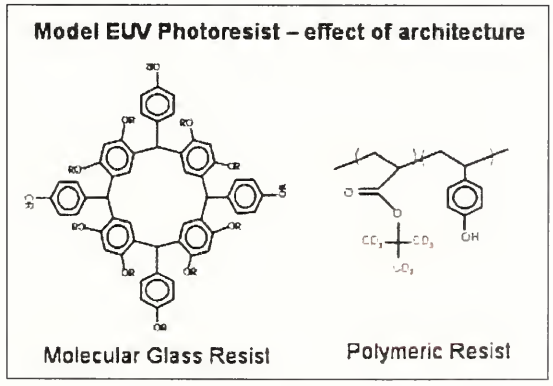


Figure 8. Two contrasting architectures of photoresist materials, but with similar chemistry: molecular glass and polymeric chemically amplified resist.

■ The Optical Technology Division is developing chemical force microscopy (CFM) to measure the surface spatial distribution of chemical species in the imaged resist. Using CFM, the homogeneity of the resist can be imaged with chemical contrast using specially prepared probe tips. This information complements the height images obtained with AFM. The distribution of PAG after exposure and deprotected polymer after PEB are of interest. The distribution of deprotected polymer is of particular interest to quantify LER by non-destructive imaging techniques at the nanometer length scale. Figure 9 shows a CFM image of an EUV-exposed PMMA thin film with 30 nm half pitch lines that has not been developed. The lighter areas are the unexposed PMMA.

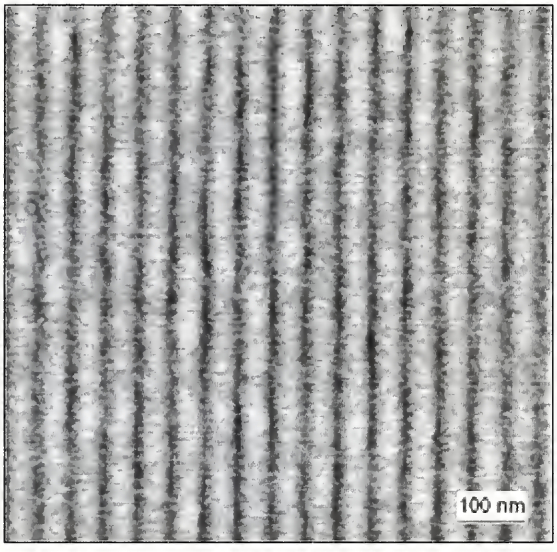


Figure 9. Chemical Force Microscopy image on an EUV imaged PMMA thin film with 30 nm half-pitch lines.

Collaborations

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DuPont Electronic Polymers L.P. – Jim Sounik, Michael T. Sheehan

Cornell University – Christopher Ober

SEMATECH – Agreement 309841 OF

Intel – CRADA 1893

Recent Publications

S. Kang, V. M. Prabhu, B. D. Vogt, E. K. Lin, W.-L. Wu, and K. Turnquest, *"Copolymer fraction effect on acid catalyzed deprotection reaction kinetics in model 193 nm photoresists,"* Proceedings of the SPIE, Vol 6153, (2006).

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B. D. Vogt, C. L. Soles, C.-Y. Wang, V. M. Prabhu, P. M. McGuiggan, J. F. Douglas, E. K. Lin, W.-L. Wu, S. K. Satija, D. L. Goldfarb, M. Angelopoulos *"Water immersion of model photoresists: interfacial influences on water concentration and surface morphology,"* Journal of Microlithography, Microfabrication, and Microsystems, 4(1), 013003 (2005).

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V. M. Prabhu, B. D. Vogt, W.-L. Wu, E. K. Lin, J. F. Douglas, S. K. Satija, D. L. Goldfarb, and H. Ito, *"Direct measurement of the counterion distribution within swollen polyelectrolyte films,"* Langmuir 74, 6647 (2005).

V. M. Prabhu and E. K. Lin, *"Advanced Measurements for Photoresist Fundamentals,"* Semiconductor Fabtech International Quarterly, 24th Edition, 99 (2004).

D. L. VanderHart, V. M. Prabhu, E. K. Lin, *"Proton NMR Determination of Miscibility in a Bulk Model Photoresist System: Poly(4-hydroxystyrene) and the Photoacid Generator, Di(t-butylphenyl) Iodonium Perfluorooctane Sulfonate,"* Chemistry of Materials, 16(16), 3074-3084 (2004).

V. M. Prabhu and E. K. Lin, *"Advanced Measurements for Photoresist Fundamentals,"* Semiconductor Fabtech International Quarterly, 24, 99-103 (2004).

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Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurement improvements have barely kept up with lithography capabilities. To maintain cost effectiveness, continued advances need to be made.

Wafer-Level and Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason, the project is presented in a number of sub-sections, each focusing on a single technology. These are:

- Scanning Electron Microscope-Based Dimensional Metrology
- Scatterometry-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials
- Optical-Based Photomask Dimensional Metrology
- Model-Based Linewidth Metrology
- Atom-Based Dimensional Metrology

Scanning Electron Microscope-Based Dimensional Metrology

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M. T. Postek

"Scanning Electron Microscopy (SEM) – continues to provide at-line and in-line imaging ... and CD measurements. Improvements are needed ... at or beyond the 65 nm generation ... Determination of the real 3-D shape...will require continuing advances in existing microscopy ..."

International Technology Roadmap for Semiconductors, 2003

Goals

Provide the microelectronics industry with highly accurate scanning electron microscope (SEM) measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage, and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors (2005) states that "Scanning Electron Microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and critical dimension (CD) measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation." The semiconductor industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 65 nm or less with a very high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size, known as CD, are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for this sub-100 nm metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project, a multidimensional project, is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for large amount of good quality samples produced inexpensively.

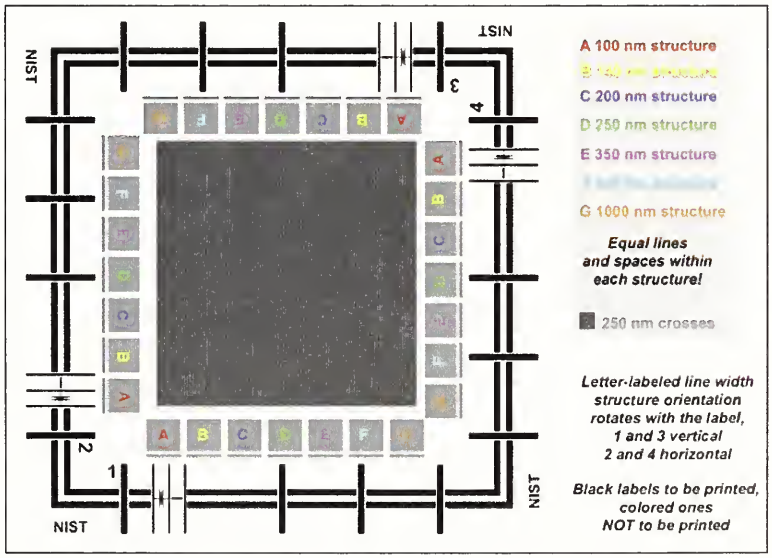

Figure 1. The final design of the SRM 2120 Magnification calibration standard reference material.

Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. In order to make this artifact available (while the final certification details are being completed) the artifact will be released as Reference Material (RM) 8120.

DELIVERABLES:

- Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask. 4Q 2007
- Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. 4Q 2007
- Upon availability of suitable quality samples, quality assessment and delivery of a batch of RM 8120. 4Q 2007
- Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples. 4Q 2007

2. SEM Performance Measurement Artifacts: This effort included the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. New methods and suitable samples are being sought to further improve this type of metrology. Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time, the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with a few nm of accuracy. In several publications, NIST demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 mm to down to 50 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

DELIVERABLES:

- Design and preparation of line width metrology artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples. 4Q 2006
- Completion of preliminary measurements on samples made by SEMATECH with the new "NIST-MAG" metrology mask. 4Q 2006

Accomplishments

■ SEM Magnification Calibration Artifacts – Samples for Reference Material 8090 have been made in the past once successfully, but later several attempts with e-beam lithography yielded no further useful samples. We now have a new, final mask designed and fabricated at International SEMATECH to get samples made by 193 nm UV light lithography. The use of this conventional lithography and a somewhat modified design provides a chance for large amount of good quality samples produced inexpensively. Because of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. There are a large number of 250 nm wide crosses for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. The fabrication of the first large batch of samples will be finished in the summer of 2006. With the arrival of the new metrology SEM these will be calibrated.

■ SEM Performance Measurements – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use.

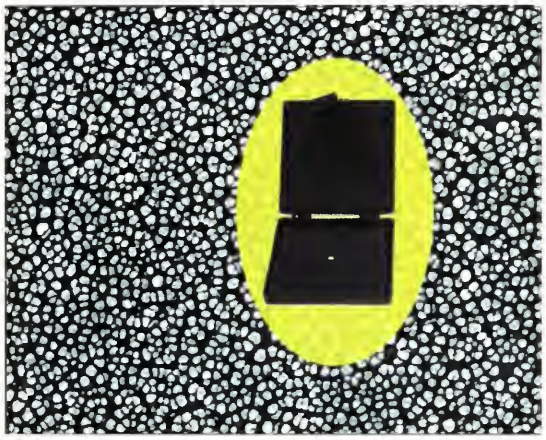

Figure 2. The RM 8091 Sharpness Reference Material.

■ SEM Linewidth Measurement Artifacts – For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view and using our high-accuracy modeling and fitting methods, a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of the SEMATECH/NIST mask has been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All of these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2007 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ Development of High Accuracy Laser Interferometer Sample Stage for SEMs – The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.04 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 3 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field of views are 2 nm by 2 nm for each images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

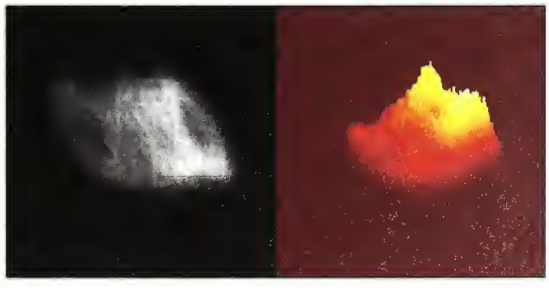

Figure 3. Short-term motion of the SEM sample stage, the stage location (left) and its density distribution during a 1 minute of dwell time, 2 nm by 2 nm field of views.

■ Development of Line Edge Roughness Metrology for Integrated Circuit Technology – The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to SEMATECH.

■ Development of Ultra-High Resolution Nano-tip Electron Gun for CD-SEMs – The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source. Nano-tips, by comparison to conventional cold field, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. Figure 4 proves that the nano-tip electron gun can deliver 6 nm resolution images while the original gun's specification for the test microscope was only 15 nm. Therefore, in an optimized electron optical column, substitution of a CFE source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size,
- Better signal-to-noise ratio and resolution, and
- Faster scan rate and better charge control.

This work has proved that nano-tips indeed improve the resolution performance of SEMs and can be used for longer periods of time. Currently further experiments are conducted to assess the optimal setting of the electron gun and the electron optical column and life time and stability parameters of the nano-tips.

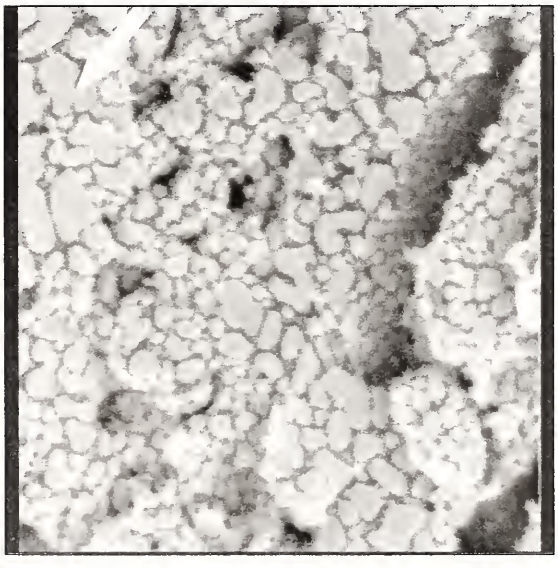

Figure 4. Nano-tip electron gun image showing 6 nm resolution taken on a gold-on-carbon resolution sample at 900 V accelerating voltage. The SEM original specification resolution is 15 nm. The field of view is 1.75 μm.

Collaborations

International SEMATECH, Advanced Metrology Advisory Group

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections

Recent Publications

A. E. Vladár, Z. Radi, M. T. Postek and D. C. Joy, *"Nano-tip Electron Gun for the Scanning Electron Microscope,"* 2006 (in press).

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M. T. Postek, and A. Vladár, *"E.Application of High Pressure/ Environmental Scanning Electron Microscopy to Photomask Dimensional Metrology,"* Characterization and Metrology for ULSI Technology (D. Seiler et al. eds) AIP Press, New York (2003).

Scatterometry-Based Dimensional Metrology

Goals

Our goals are: (1) increase the effectiveness of scatterometry and other optical critical dimension (OCD) methods by providing industry with new measurement techniques, improved modeling, and standards; (2) provide assessments of accuracy and sensitivity of various OCD methods; and (3) develop facilities to accurately assess OCD targets. Develop improved OCD methods for assessing critical dimension and overlay.

Customer Needs

Scatterometry is increasingly becoming a preferred method for online critical dimension (CD) metrology. The method relies upon measurements of the reflectance or diffraction of small test grating structures as functions of angle, wavelengths, and/or polarization. By comparing measurement results with an extensive library of theoretical simulations, tools can extract such line profile parameters as critical dimension, sidewall angle, and height, as well as more detailed descriptions of the sidewall shape.

While scatterometry has gained significant acceptance, it is continuing to grow in utility. However, there are many issues that remain that prevent it from having absolute accuracy. For example, the effects of finite illumination, finite target array size, line-edge and line-width roughness, uncertainties in the optical properties of the materials in the structure, neglect of surface oxides or other layers, radiometric accuracy, and the integrity of the theoretical model all contribute to the final measurement uncertainty in ways that are at this time poorly understood.

Ultimately, the industry needs reference artifacts that can test the validity of the results obtained by scatterometry tools. Such an artifact might consist of a set of gratings that have been characterized by a variety of techniques, including scatterometry, scanning electron microscopy (CD-SEM), atomic force microscopy (CD-AFM), and transmission electron microscopy (TEM). Scatterometry provides an independent method compared to the others, and if a comprehensive uncertainty budget were developed for the method, it would substantially improve the overall state of dimensional metrology.

Technical Strategy

There are three major strategies for improving the effectiveness of scatterometry. One strategy is to develop efficient models for the diffraction of light by structures on surfaces, so that NIST has state-of-the-art capabilities to perform scatterometry measurements and analysis as well as to provide standard data for a variety of model structures. The second strategy is to assess the sensitivity and accuracy of scatterometry methods to different structures, in order to provide industry with an understanding of what determines the ultimate sensitivity and accuracy of the methods. Finally, the third strategy is to develop in-house measurement capabilities with the long-term goal to perform scatterometry measurements on reference materials, to perform inter-laboratory comparisons, and to further develop the scatterometry technique.

Specific project elements are defined below:

1. Theoretical Scatterometry Modeling – Rigorous coupled wave (RCW) based theories are the most common methods used to analyze scatterometry data. We have developed in-house capability to perform RCW calculations from arbitrary two-dimensional periodic structures consisting of isotropic materials. These codes are being used to generate libraries for profile extraction as well as test calculations to assess the sensitivity of scatterometry to changes in model parameters or to non-ideal target profiles. Extensions to this capability are required to assess the effects of line-edge and line-width roughness and material anisotropy, as well as to perform RCW calculations on three-dimensional structures. Building upon the SCATMECH library of codes that have been made available on the web for diffuse scattering calculations, we intend to publish these codes.

DELIVERABLES:

- Publication of theory for anisotropic lines. 3Q 2006
- Publication of two-dimensional RCW code in the SCATMECH library. 1Q 2007
- Publication of three-dimensional RCW code in the SCATMECH library. 1Q 2008

2. Assessment of Accuracy and Precision of Scatterometry – Scatterometry relies heavily on prior knowledge of the specific structure being examined. For example, optical properties of all incorporated materials are required for the

Technical Contact:
T. Germer

simulations. Reasonable parameterization of sidewall profiles are required to yield meaningful profiles. Two dimensional structures are assumed to not exhibit line-edge or line-width roughness. In this program element, we are assessing the impact that each model parameter has on the outcome of the measurement. The goal is to establish an independent uncertainty budget that includes all sources of random and systematic uncertainties. Furthermore, we are assessing the sensitivity limits of scatterometry, to determine how far into the future scatterometry tools can provide critical dimension metrology.

DELIVERABLES:

- Perform study of the limits of scatterometry precision for simple gate and gate-resist gratings. 1Q 2006
- Assess effects of line-edge and line-width roughness using random 2-D gratings. 3Q 2006
- Perform study of the limits of scatterometry precision for metallic lines and complex sidewall profiles. 1Q 2007
- Develop method for assessing uncertainty arising from uncertainty in material optical constants. 1Q 2007

3. Scatterometry Measurements – We are developing a new instrument, based upon the currently existing laser-based Goniometric Optical Scatter Instrument (GOSI), Fig. 1, used for diffuse scatter measurements, to perform scatterometry measurements on industry-relevant targets on 300 mm wafers. The measurement capability will include angle-scanned scatterometry at a number of discrete laser wavelengths. This instrument will have the capability to perform conical scatterometry measurements and will be used to perform traditional measurements as well as measurements of higher-order, non-specular diffraction and diffuse scatter. A long term goal is to develop reference scatterometry targets, measure them with this instrument, provide accurate determinations of their dimensions and profiles, and have an uncertainty placed on the results. Another long term goal is to develop novel measurement modalities that improve the utility of scatterometry. One method we have demonstrated is microscope-based scatterometry using back focal plane imaging. This technique enables collection of multiple diffraction order scatterometry signatures in a single image, can be configured for both dense and isolated targets, and allows scatterometry and image-based metrology to be performed on the same tool.

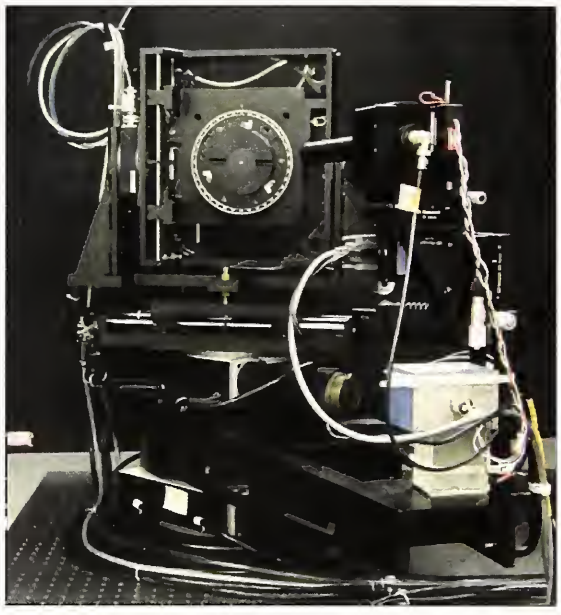

Figure 1. The Goniometric Optical Scatter Instrument (GOSI) is a reference reflectometer for diffuse and specular scattering measurements.

DELIVERABLES:

- Perform initial scatterometry measurements using current instrumentation. 1Q 2006
- Complete construction of new scatterometer and benchmark its performance. 4Q 2006
- Perform measurements on potential reference scatterometry target. 4Q 2006

Accomplishments

■ We have developed efficient rigorous coupled wave (RCW) software for two-dimensional periodic structures in the conical geometry. Results of the in-house code have been compared with finite difference time domain, surface integral equation, and other RCW implementations. This software is also configured to run on a large cluster computer, so that library generation is possible.

■ As part of our effort in assessing the precision and accuracy of scatterometry, we have performed a study of the sensitivity of scatterometry to CD and sidewall angle for a large number of different measurement modalities, including angle-scanned and wavelength-scanned reflectometry and ellipsometry, for amorphous silicon gate and gate-resist structures. This study included parameters appropriate from the 45 nm half-pitch node to the 18 nm half-pitch node. The results (see Fig. 2) demonstrated that scatterometry can achieve the necessary sensitivity to measure dense gratings at these nodes. Future work, however, will be necessary to achieve sufficient sensitivity to isolated features.

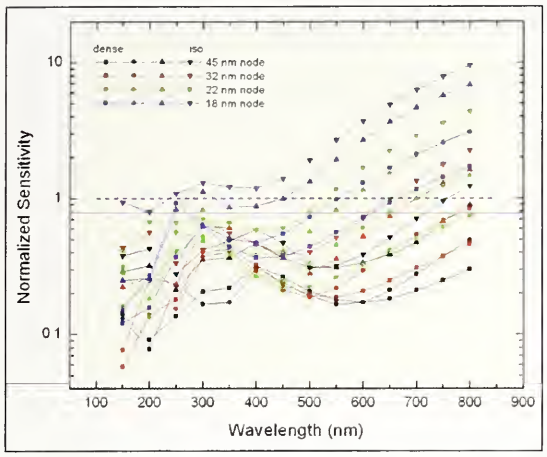

Figure 2. Estimated bottom dimension sensitivity, normalized by the 2 % of bottom dimension specification, calculated for gate gratings measured by angle scans of the reflected Stokes parameters with angles less than 70°.

■ In the area of scatterometry measurement, we have demonstrated angle-resolved scatterometry using back-focal-plane imaging in a microscope (see Fig. 3). By using suitable selection of the illumination angles, we measured the scatterometry signatures of targets with only specular reflectance (grating pitch 300 nm) and those with both specular and higher-order diffraction (grating pitch 600 nm). Targets with line widths of 146 nm to 158 nm (as measured by SEM) were investigated, and the measurement was shown to have nanometer-level sensitivity to line width. Initial generation of RCW libraries and extraction of target parameters from the libraries is underway, as is comparison of these parameters with measurements made by SEM and AFM.

Figure 3. Image of the back focal plane of a microscope with a tilted slit illumination, showing angle-resolved specular (zero order, longer line) and diffracted (first order, shorter side lines) efficiencies.

Collaborations

International Sematech Manufacturing Initiative, Benjamin Bunday, Limits of Scatterometry Study.

Department of Electrical Engineering, Texas A&M University, Professor Krzysztof Michalski, Modeling of Scattering by Lines Having Anisotropic Optical Properties.

Recent Publications

Thomas A. Germer and Egon Marx, "Simulations of Optical Microscope Images," in Metrology, Inspection, and Process Control for Microlithography XX, C.N. Archie, Ed. Proc. SPIE **6152**, in press (2006).

Heather J. Patrick, Ravikirin Attota, Thomas A. Germer, Michael Stocker, Richard M. Silver, "Scatterfield microscopy using conventional and back focal plane imaging with an engineered illumination field," in Metrology, Inspection, and Process Control for Microlithography XX, C.N. Archie, Ed. Proc. SPIE **6152**, in press (2006).

R. M. Silver, R. Attota, M. Stocker, M. Bishop, L. Howard, T. Germer, E. Marx, M. Davidson, and R. Larrabee, "High-resolution optical metrology," in Metrology, Inspection, and Process Control for Microlithography XIX, R.M. Silver, ed., Proc. SPIE **5752**, 67–79 (2005).

Ravikiran Attota, Richard M. Silver, Thomas A. Germer, Michael Bishop, Robert Larrabee, Michael T. Stocker, and Lowell Howard, "Application of through-focus focus-metric analysis in high resolution optical metrology," in Metrology, Inspection, and Process Control for Microlithography XIX, R.M. Silver, ed., Proc. SPIE **5752**, 1441–1449 (2005).

Scanning Probe Microscope-Based Dimensional Metrology

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in scanning probe microscope-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2005 edition, the goal in 2006 for critical dimension (CD) measurement precision for isolated lines was ± 0.58 nm; this demand tightens to ± 0.29 nm by 2012.

Although most in-line metrology is performed using scanning electron microscope (SEM) and scatterometry, these instruments are not presently capable of first-principles accuracy. That is, they must be calibrated using reference measurements from a tool or combination of tools which is capable of intrinsic accuracy. Such a tool is now referred to as a reference measurement system (RMS), and the 2005 edition of the *ITRS* highlights the growing importance of an RMS. The use of atomic force microscope (AFM) and transmission electron microscope (TEM) cross section for this purpose – often in combination – is now a fairly common practice in the industry.

The technical focus of this project, development and implementation of scanned probe microscope instrumentation for traceable dimensional metrology, is thus driven by the anticipated industry needs for reduced measurement uncertainty for in-line metrology tools such as the SEM and scatterometer – since these in turn rely on reduced measurement uncertainty for techniques such as AFM that are often implemented as an RMS.

Customer Needs

The SEM is still the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scatterometry or optical critical dimension (OCD) metrology is also rapidly gaining acceptance as an in-line process metrology tool. Scanning probe microscopes (SPMs) possess unique capabilities, which may significantly enhance the performance of SEMs for in-line CD measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, the availability of traceable pitch, height, and width standards in this regime is limited.

Technical Strategy

The SPM dimensional metrology program consists of three inter-related thrusts: The first two thrusts address SPM dimensional metrology with two in-house research instruments at NIST, and the third thrust involves a partnership with SEMATECH to maintain traceability on a commercially available in-line SPM housed in the manufacturing facility at SEMATECH. The two instruments housed at NIST are a calibrated atomic force microscope (C-AFM) for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width.

The C-AFM is a custom built instrument that has metrology traceable to the wavelength of light for all three axes of motion, and it has provided calibrated pitch and height measurements for a variety of nano-scale applications. Pitch measurements in the micrometer regime and below can currently be performed with relative standard uncertainties as low as 5×10^{-4}, and step height measurements up to several hundred nanometers can be performed with a relative standard uncertainty approaching 1×10^{-3}. The C-AFM has participated in two international comparisons of sub-micrometer pitch measurements and one comparison of step height measurements.

DELIVERABLES:

- Completed 2-dimensional pitch measurements using C-AFM as NIST participation in NANO5 – an International Supplementary Key Comparison in Nanometrology. 1Q 2006
- Performed extensive CD-AFM measurements, using the SXM320 at NIST, on next generation single crystal critical dimension reference material (SCCDRM) samples for phase 1 of the process optimization experiment in collaboration with EEEL and ITL. 2Q 2006

Technical Contacts:
R. Dixson
G. Orji
T. Vorburger
J. Fu

- Presented two papers on AFM dimensional metrology at SPIE Microlithography meeting – covering all three of the project thrusts: the C-AFM, the CD-AFM at NIST, and the CD-AFM reference measurement system (RMS) at SEMATECH. 2Q 2006
- Using the SXM320 at NIST, perform measurements on final phase next generation SCCDRM samples as prototypes for a potential SRM. 4Q 2006
- Perform additional SXM trial measurements of pitch and height on OMAG3L wafer to determine the SXM performance as a comparator for support the prototype SRM2089 wafer. 4Q 2006

The second and third thrusts involve the most commonly used AFM-based method of linewidth metrology in industry: CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. The SXM320 is a prior generation commercially available CD-AFM. Initially, this instrument was used to implement the CD-AFM RMS at SEMATECH during the tenure of Ronald Dixson as the first NIST Guest Scientist there. Now that the instrument is housed at NIST, the uncertainties have been further refined. Currently, pitch measurements can be performed with a relative standard uncertainty of approximately 2×10^{-3}. Step height measurements have a relative standard uncertainty 4×10^{-3}, and linewidth measurements can have standard uncertainties as low as 1 nm. This is a result of the most current release of NIST single crystal critical dimension reference materials (SCCDRM) that was completed in 2005.

The third thrust involves collaboration with SEMATECH to maintain a traceable CD-AFM (RMS) in the manufacturing facility there. This thrust is currently overseen by George Orji who is now the second NIST Guest Scientist at SEMATECH. A current generation CD-AFM, the Veeco Dimension X3D, is now being used to implement the RMS. As is true for the SXM at NIST, the SCCDRM project has resulted in the ability to perform linewidth measurements with a standard uncertainty of 1 nm. The relative uncertainties in pitch and height measurements have been recently reduced to 1×10^{-3} and 2×10^{-3}, respectively.

DELIVERABLES:

- Implement new SPC monitoring procedure for CD-AFM RMS at SEMATECH using secondary sites on the SCCDRM L4 chip that serves as system monitor. 1Q 2006
- Complete a detailed study of higher order tip effects in CD-AFM metrology and publish peer reviewed journal article on the results. 3Q 2006

Accomplishments

■ The NIST/SEMATECH partnership in advancing AFM metrology in semiconductor manufacturing continues. George Orji is now in the second year of his tenure as the second NIST Guest Scientist at SEMATECH, following a three year tenure of Ronald Dixson as the first NIST Guest Scientist there. George has continued the NIST engagement with SEMATECH by supporting their SEM benchmarking activities with the RMS, and he has overseen the reduction of pitch and height uncertainties by approximately a factor of two.

■ We are collaborating with other NIST researchers and external partners such as SEMATECH to develop linewidth standards. A major component of this effort has been the single crystal critical dimension reference materials (SCCDRM) project initiated by NIST researchers in EEEL (Cresswell and Allen). In late 2004, we completed a release of SCCDRMs to SEMATECH and its member companies, and CD-AFM dimensional metrology played a central role. The measurements on the SCCDRM samples were performed by NIST scientist Ronald Dixson using the X3D at SEMATECH which had been implemented as a CD-AFM reference measurement system (RMS) for traceable measurements of pitch, height, and width. High resolution transmission electron microscopy (HRTEM) was used as an indirect method of tip width calibration for the SCCDRM samples. The AFM and HRTEM results that were used for the tip calibration are shown in Fig. 1. Features on the distributed samples ranged in width from approximately 50 nm to 250 nm with expanded uncertainties of about 2 nm ($k = 2$) on most features.

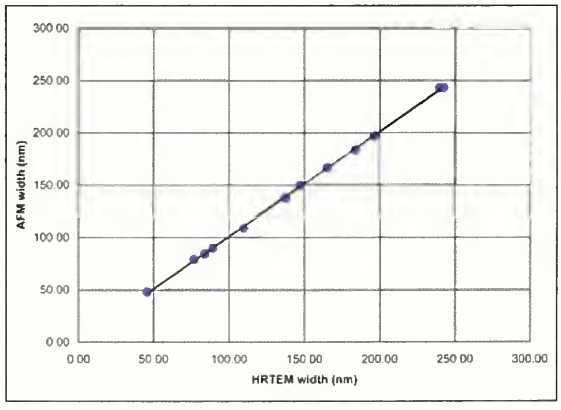

Figure 1. Regression of CD-AFM width values on HRTEM values. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to correct the tip width calibration.

■ As a result of this project, CD-AFM linewidth measurements can now be performed with a 1 nm (k = 1) standard uncertainty. This standard for width calibration is now being used on both the X3D and the SXM at NIST. An image of an SCCDRM taken on the SXM320 is shown in Fig. 2. In 2005, we launched the "next generation" of the SCCDRM project and are currently performing a series of designed experiments to further improve the performance characteristics of the SCCDRMs – including linewidth uniformity. In the first phase of these experiments, we have observed feature widths as low as 20 nm with uniformity at the 1 nm level.

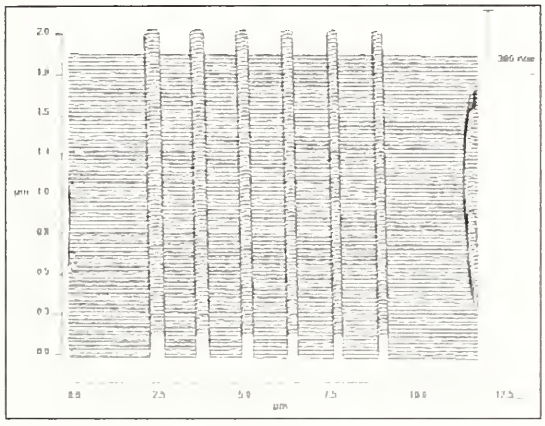

Figure 2. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration. Measurements performed by R. Dixson, sample developed by M. Cresswell and R. Allen.

■ We have used the C-AFM to participate in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of traceable measurements of dimensional quantities important to the semiconductor industry. We have previously participated in comparisons of step height and one dimensional pitch measurements. The results of these comparisons have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. During 2005, we participated in a comparison of two dimensional pitch measurements: the C-AFM was used to measure both a 300 nm and 1000 nm grating. An example of a C-AFM image on the 1000 nm grating is shown in Fig. 3. A similar comparison of linewidth measurements is currently being planned and will be led by NIST.

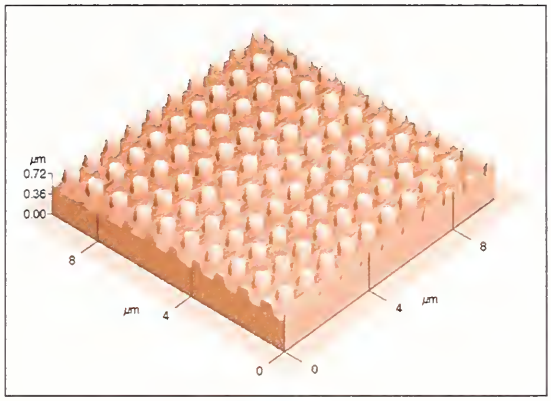

Figure 3. An image of a 1000 nm pitch grating taken using the C-AFM as part of an international comparison of two dimensional pitch measurements.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2004 we developed a draft standard for AFM z-calibration using the single atom steps for the ASTM Subcommittee E42.14 on STM/AFM. This draft standard is still being revised and undergoing review within the subcommittee.

■ We are also developing a technique for AFM linewidth metrology based on image stitching. This involves the acquisition of paired images using a carbon nanotube probe. The nanotube tip enables data acquisition at high resolution on one side of the line in each image, and the specimen is rotated 180 degrees between the two measurements. Stitching these two images into a composite offers the potential of accurate linewidth metrology. We have completed two generations of an experiment in which the stitching result is compared with CD-AFM. The composite image used in one of our published comparisons between image stitching and CD-AFM is shown in Fig. 4 (page 36). Currently, we are assessing the uncertainties and continuing to develop this approach.

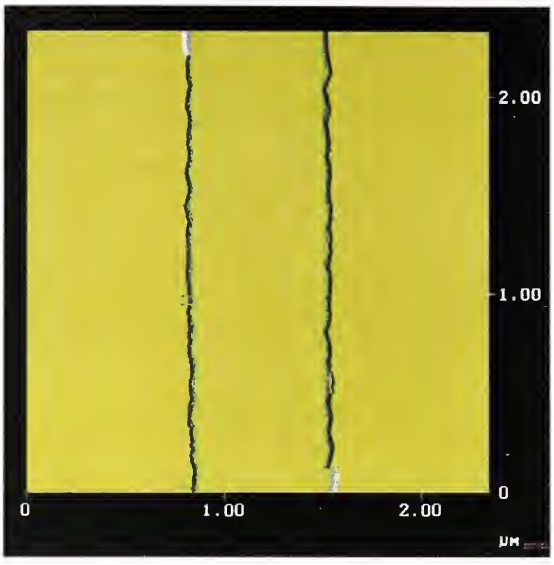

Figure 4. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.

- We continue to refine the CD-AFM RMS at SEMATECH and bring its traceable measurement capabilities to bear on semiconductor manufacturing applications. During the tenure of both NIST Guest Scientists at SEMATECH, we have used this RMS system to provide reference metrology for both SEM and scatterometer benchmarking, measurements of SEM-induced shrinkage of 193 nm photoresist, and to provide reference metrology for evaluation of several new optical methods for measurement of photomasks.

- In the SEM benchmarking applications, our basic methodology is to perform both CD-AFM and SEM measurements on a series of features on a focus exposure matrix that spans a process window. This approach means that both tools see features that have a range of widths as well as secondary characteristics such as sidewall angle and corner rounding. A regression of the AFM/SEM data allows the SEM to be checked for bias, scale calibration, and linearity of response across the FEM. An example of a SEM/AFM regression using measurements of isolated polysilicon lines is shown in Fig. 5. SEMATECH and its members place high value on SEMATECH's tool benchmarking activities and the support these activities receive from the NIST-supported CD-AFM RMS.

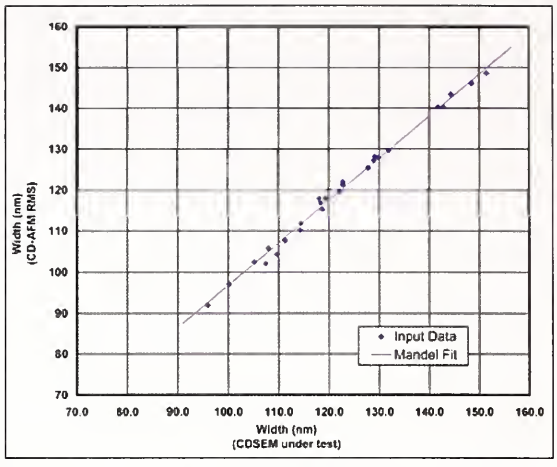

Figure 5. An example of an AFM/SEM regression performed as part of a SEMATECH benchmarking activity during the tenure of Ronald Dixson as the first NIST Guest Scientist at SEMATECH. The measurements were performed on isolated etched polysilicon lines that spanned a wide process window focus exposure matrix. The Mandel regression allows for uncertainty in both variables and is the most appropriate way to compare a tool under test with the reference measurement system. In this example, the SEM performance is very good and exhibits a bias of only 3 nm and linearity within the uncertainties of the comparison.

Collaborations

SEMATECH, Austin TX

Veeco Metrology, Santa Barbara CA

IBM Burlington, VT

IBM Almaden Research Center, San Jose, CA

ELORET Corp./ NASA Ames Research Center, Moffett Field CA.

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China.

Recent Publications

R. Dixson, N.G. Orji, J. Fu, M. Cresswell, R. Allen, W. Guthrie, *"Traceable Atomic Force Microscope Dimensional Metrology at NIST,"* to be published in Proc. SPIE 5752, (2006).

N. Orji, A. Martinez, R. Dixson, J. Allgair, *"Progress on Implementation of a CD-AFM based Reference Measurement System,"* to be published in SPIE Proceedings Vol. 6152 (2006).

R. G. Dixson, R. A. Allen, W. F. Guthrie, and M. W. Cresswell, *"Traceable Calibration of Critical-Dimension Atomic Force Microscope Linewidth Measurements with Nanometer Uncertainty,"* J. Vac. Sci. Technol. B Vol. 23, 3028-3032 (2005).

J. Fu, R. Dixson, N. Orji, T. Vorburger, C. Nguyen, *"Linewidth Measurement from a Stitched AFM Image,"* AIP Conference Proceedings, Vol. 788, 421-426 (2005).

R. Dixson, J. Fu, N. Orji, W. Guthrie, R. Allen, M. Cresswell, *"CD-AFM Reference Metrology at NIST and SEMATECH,"* SPIE Proceedings Vol. 5752, 324-336 (2005).

M. Cresswell, R. Dixson, W. Guthrie, R. Allen, C. Murabito, B. Park, J. Martinez de Pinillos, and A. Hunt, "Critical Dimension Reference Features with Sub-Five Nanometer Uncertainty," *SPIE Proceedings* Vol. 5752, 288-303 (2005).

N. G. Orji, M.I. Sanchez, J. Raja, and T. Vorburger, "AFM Characterization of Semiconductor Line Edge Roughness," in *Applied Scanning Probe Methods*, edited by B. Bhushan, H. Fuchs, and S. Hasaka (Springer Verlag, Berlin, 2004) p. 273.

B. D. Bunday, M. Bishop, D. McCormack, J. S. Villarrubia, A. E. Vladar, R. Dixson, T. Vorburger, N. G. Orji, J. A. Allgair, *"Determination of Optimal Parameters for CD-SEM Measurement of Line Edge Roughness,"* Proc. SPIE 5375, (2004).

R. Dixson and A. Guerry, *"Reference Metrology Using a Next generation CD-AFM,"* Proc. SPIE 5375, 633 (2004).

X. Zhao, J. Fu, W. Chu, C. Nguyen, and T. Vorburger, *"An Image Stitching Method to Eliminate the Distortion of the Sidewall in Linewidth Measurement,"* Proc. SPIE 5375, 363 (2004).

Small Angle X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
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E. K. Lin
W. L. Wu

Goals

To develop a small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. Further, the wavelengths utilized by SAXS based measurements well complement current metrology tools based on optical scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the production of standards for current industrial solutions such as CD-SEM.

Technical Strategy

1. Exposure systems capable of sub-50 nm patterning are expected by 2009, requiring control of CD on the level of nanometers and in some cases sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of Angstrom level precision in critical dimension evaluation over large (50 µm x 50 µm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission (see Fig. 1) using a sub-Angstrom wavelength. The high energy of the X-ray source allows the beam to pass through a production quality silicon wafer, and could become amenable to process line characterization. The measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors are sufficient to implement a laboratory scale device capable of high precision measurements. This year, NIST has designed and installed the world's first laboratory scale CD-SAXS device.

DELIVERABLES: Evaluate laboratory scale CD-SAXS instrument. 4Q 2006

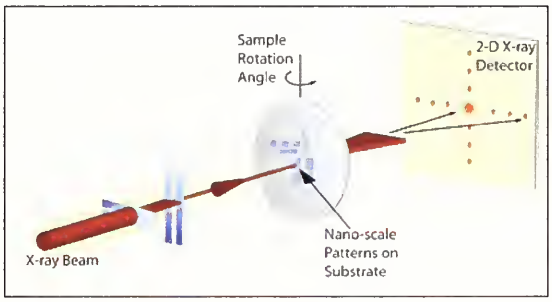

Figure 1. Schematic of the SAXS transmission geometry. Shown is the X-ray beam as it passes through the patterned sample and scattered at an angle 2θ. For a precisely aligned sample with known composition, a 3-D lineshape is obtained in one transmission measurement. Unknown samples can also be characterized through measurements at a variety of sample angles.

2. Characterization of pattern quality includes shape factors such as the sidewall angle and curvature. Measurements taken at a series of angles of incidence allows the reconstruction of the line shape. We have performed tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1 degree. Ongoing analysis and technique refinement will provide additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition to a "high speed," model dependent characterization performed in a single measurement, a second method will be developed based on measurements at multiple sample orientations. This method

provides a more precise measurement of the entire pattern cross section in a non-destructive and model independent manner (see Fig. 2). In the current technology node, this measurement can be used to evaluate optical scatterometry models for line shape, while providing a general capability to measure a pattern of arbitrary cross section in future technology nodes.

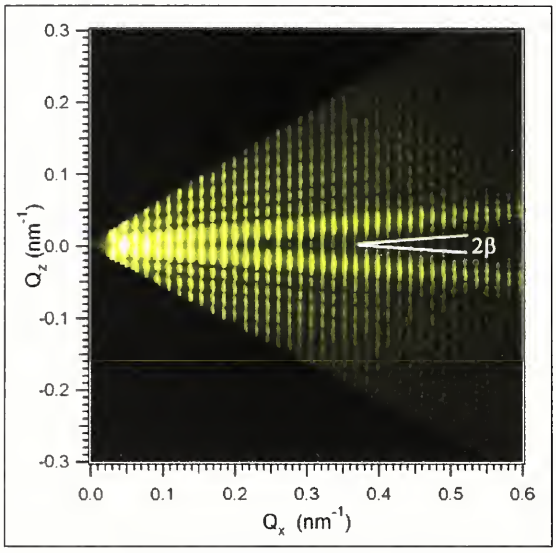

Figure 2. Data from measurements of a polysilicon line grating at varying sample angles. Shown is a contour plot of diffracted intensity as a function of scattering vectors parallel to the substrate, Qx, and normal to the substrate, Qz. The sidewall angle, β, is the half angle of the prominent ridges.

3. Current LER and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Techniques such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of optical scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. In cooperation with the Advanced Metrology Working Group at SEMATECH, NIST has designed a series of structures to model different types of roughness. CD-SAXS data from these structures will help further develop modeling protocols.

DELIVERABLES: Quantify sidewall roughness originating from standing waves during photoresist imaging with CD-SAXS. 3Q 2006

DELIVERABLES: Provide measurement of model LER model structures with CD-SAXS. 4Q 2006

4. As circuit designs increase in complexity, next generation measurement methods must be capable of characterizing patterns that deviate substantially from line/space patterns. As an example, a capability to precisely characterize dense arrays of high aspect ratio vias non-destructively is needed. The use of a 2-D collimated beam and a 2-D detector in the CD-SAXS technique provides a natural capability to characterize patterns such as vias, posts, and via pads. While the capability to observe such structures has previously been demonstrated, routine analysis of this class of structures has not been achieved. Using a series of patterns including vias of diameter less than 60 nm, we are developing specific experimental protocols, extending those developed for line/space patterns, to provide a data set capable of describing a precise pattern shape in 2-D arrays of patterns.

DELIVERABLES: Provide measurements and model describing the measurement of 2-D arrays of 60 nm via patterns. 4Q 2006

5. CD-SAXS measurements can be applied towards several other important problems for both semiconductor and next-generation nanofabrication technologies. CD-SAXS measurements are being evaluated as a potential measurement method capable of determining the densification of the sidewall of plasma etched, patterned nanoporous low-κ dielectric films. Electron microscopy has been used, but has been unable to measure the densification profile with sufficient resolution. In addition, CD-SAXS measurements can be used to evaluate the fidelity of pattern transfer with the nanoimprint lithography (NIL). In NIL, the pattern from a hard, master mold is transferred into an underlying organic material through mechanical pressure and elevated temperature or curing with ultraviolet light. CD-SAXS measurements of both the mold and the resulting pattern can be compared to evaluate the quality of the NIL structure.

DELIVERABLES: Demonstrate SAXS measurement methods for sidewall damage characterization in plasma etched patterned low-κ dielectric materials. 3Q 2006

Accomplishments

- We have provided the first measurements of sidewall angle using small angle X-ray scattering (SAXS). Using a series of photoresist gratings produced at the IBM T. J. Watson Research Center (Q. Lin), CD-SAXS was performed using at the Advanced Photon Source (Argonne National Laboratory) to measure photoresist patterns with

well-defined sidewall angles. The protocol involves measurements of the sample over 20 degrees of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle (see Fig. 2). The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol can be adopted for other pattern shapes.

- Demonstrated a capability to measure correlated fluctuations in line edge position using CD-SAXS measurements of a series of line/space patterns in a "193 nm" photoresist produced at IBM T. J. Watson Research Center (A. Mahorawala) (see Fig. 3). These samples are believed to possess systematic, small shifts in the pattern. These shifts provide insight into measurements of line edge roughness (LER) where the roughness is highly correlated. The resulting data shows distinct streaks of intensity emanating from the diffraction peaks, particularly strong in the lower order peaks. These represent the first evidence of a capability of CD-SAXS to measure different types of defects related to the overall line edge roughness.

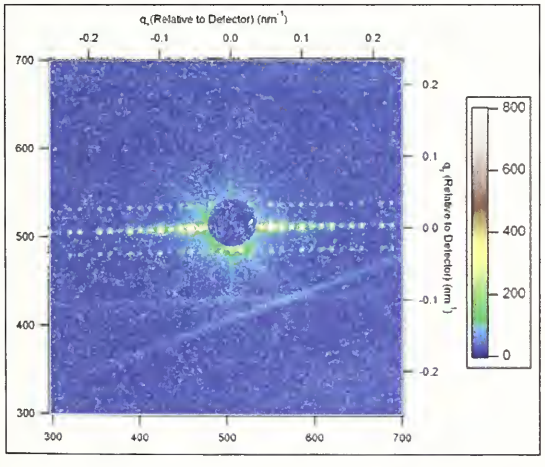

Figure 3. Detector image of etched polysilicon lines with designed line edge roughness. In addition to the typical diffraction spots characterizing pitch and linewidth, satellite peaks of intensity are observed symmetrically above and below the main diffraction axis. The additional peaks are a result of correlated sidewall roughness.

- Demonstrated a capability to measure a dense array of vias where the diameter of the vias were etched into a plastic substrate are less than 60 nm (see Fig. 4). Vias were etched into a produced into a plastic substrate at the IBM Almaden research center (M. Sanchez). The result demonstrates the capability of CD-SAXS to probe dense vias of sub-100 nm size. Ongoing work will attempt to provide a protocol for the evaluation of the full 3-D via shape as demonstrated for line/space patterns.

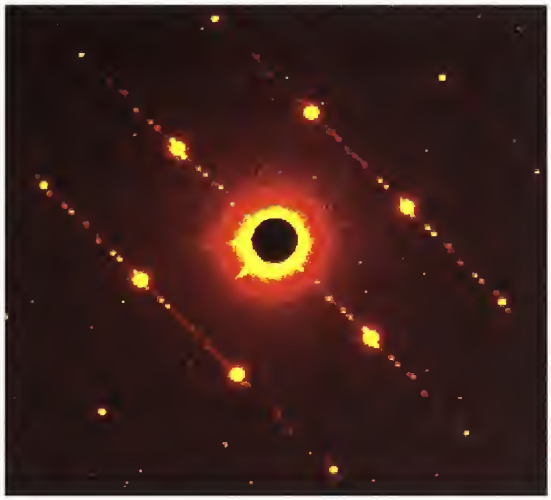

Figure 4. CD-SAXS detector image resulting from a dense array of 60 nm vias. The array of diffraction patterns suggests an approximately hexagonal packing of the vias.

- Initial feasibility studies have demonstrated the potential of CD-SAXS to detect and to estimate the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

- The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height, and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature

(T_G). Heating these patterns below T_G does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above T_G, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

Collaborations

Polymers Division, MSEL, Chengqing Wang, Derek L. Ho, Christopher L. Soles, Hyunwook Ro, Yifu Ding

Intel Corporation, Kwang-Woo Choi, Bryan Rice, sub-50 nm structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

SEMATECH, Youfan Liu, Metrology of low-κ patterns using CD-SAXS.

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

University of Michigan, Stella Pang, Nanoimprinted polymeric structures.

Molecular Imprints, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

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T. Hu., R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, D. Keane, S. Weigand, J. Quintana "Small angle X-ray scattering metrology of side wall angle and cross section in nanometer scale gratings," J. Appl. Phys. 96, 1983 (2004).

R. L. Jones, T. Hu, E. K. Lin, W. L. Wu, R. Kolb, D. M. Casa, P. J. Bolton, and G. G. Barclay, "Small angle X-ray scattering for sub-100 nm pattern characterization," Appl. Phys. Lett., 83, 4059 (2003).

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Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Technical Contact:
M. W. Cresswell

Goals

The goal of this project is to develop test-structure-based reference materials with emphasis on supplying road-map-compliant physical standards for critical-dimension (CD) metrology-tool development and calibration and to contribute to organizations supporting the development of CD metrology standards for the semiconductor industry. The specific near-term goal is fabricating a quantity of CD reference-features with nominal CDs in the range 20 nm to 160 nm and having 2σ (expanded uncertainties) of less than 2 nm by July 2006.

Customer Needs

The Semiconductor Industry Association's International Technology Roadmap for Semiconductors states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of gate microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that the situation can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. The technology that the project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation.

Further details of customer needs that have been identified since the SCCDRM distribution to SEMATECH Member Companies in January 2005, and now impact the project's responding technical strategy, are described in the next section.

Technical Strategy

The fundamental SCCDRM technical strategy is to pattern Silicon on Insulator (SOI) device layers with lattice-plane selective etches of the kind used in silicon micro machining, which provides reference features with quasi-atomically planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the implementation include starting silicon SOI wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining. However, the difficulty of obtaining satisfactory SOI material in larger diameters is driving us towards a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and originates with measurement of a selection of reference-feature CDs with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression of the each CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by, in this case, AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in Fig. 1 (page 44). To maintain maximum possible accuracy in the transfer-metrology operation, an elaborate reference-feature selection protocol has been established to identify

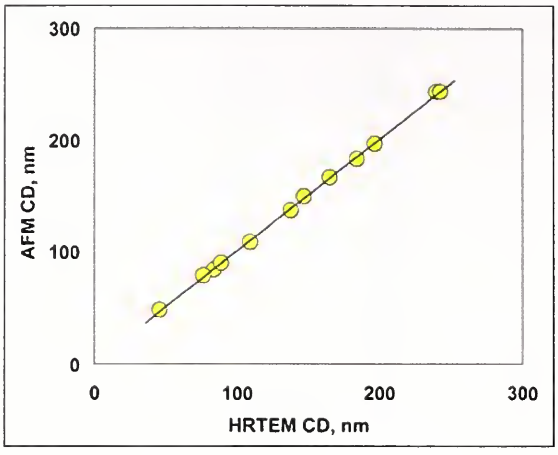

Figure 1. Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

reference features that qualify by virtue of their CD-uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to etched CDs of between 50 nm and 300 nm. The "best" 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20K magnification to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25 nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs — typically less than 150 nm. Candidate AFM targets so identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a *calibration* sub-set and a *product* subset. All six features of the selected targets on the chips on the calibration sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation. Since such operations are very costly, this capability is economically advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range.

Since 200 mm (110) starting material is unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in Fig. 2. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The chips that were delivered in January 2005 were mounted in 200 mm carrier wafers for distribution.

The Project's technical strategy is now evolving in a way that is addressed in the material that follows below. In summary, it is responding to industry push to implement measures that make the SCCDRMs more compatible with end-user requirements. These measures include:

- replacing the carrier-wafer with a monolithic 200 mm wafer implementation,
- replacing the buried oxide of SOI wafers with a buried boron diffusion having an epitaxial silicon layer deposited over it,
- further reducing the CDs of calibrated features to 20 nm and the uncertainties of the calibrated CD to less than 1.0 nm,
- improving the reference feature's CD uniformity to enable certifying the CD of an extended length,
- improved on-wafer navigation for the end user convenience,

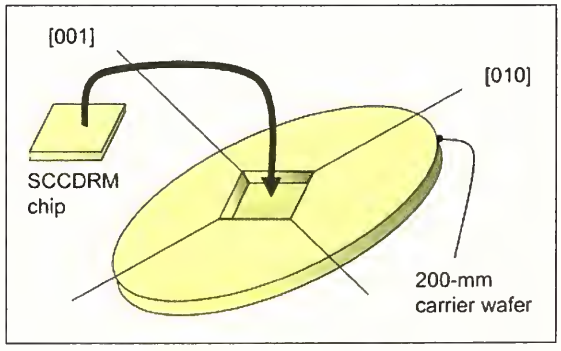

Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

- calibrating a selection of OCD gratings that are replicated at the same time as the isolated lines that have been supplied so far, and
- improved management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and to some extent adversely affect the uncertainty values of the delivered product.

Implementing these aggressive measures requires wafer-processing facilities that require innovative teaming with other laboratories. Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials. Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials.

DELIVERABLES:

- Conclusion and reporting of the screening experiment to identify which combinations of six pattern-transfer process factors drive down reference feature CDs and their uncertainties. 4Q 2006
- Patterning and metrology of trenches patterned into a (110) SOI device layers for their evaluation as micro fluidic channels for MEMS-based bio-applications having otherwise unavailable requirements. 4Q 2006
- Devising a hybrid optical-EB-direct-write lithography-process to pattern a selection of 200 mm bulk-silicon (110) wafers with SCCDRM test structures with CDs at or below the 20 nm level. 1Q 2007
- Applying 193 nm lithography to the patterning of a selection of 200 mm bulk-silicon (110) wafers with a SCCDRM test structures having reference-feature CDs at or below the 20 nm level. 3Q 2007
- Extend measurements, analyses, and evaluation of the application of SEM-CD measurements as a SCCDRM transfer metrology. 3Q 2006
- Fabricate and evaluate a selection of OCD grids patterned on SCCDRM wafers as an optical-CD reference material. 3Q 2006
- Initiate the implementation of a plan to fabricate and calibrate a selection of isolated-line CD-SRMs. 4Q 2006

DELIVERABLES: Reduce reference-feature sidewall asperities by developing separate processes that target sidewall contamination by organic materials and by residual moisture. These processes may include immersion of the patterned chips in ultra-sonically agitated solvents, extensive pre-cleaning of quartz-ware, and vacuum baking. 2Q 2006

Accomplishments

■ This project, in collaboration the NIST Precision Engineering and Statistical Engineering Divisions, has recently designed and implemented a screening experiment to identify which combinations of six pattern-transfer process factors drive down reference feature CDs and their uncertainties. A 2^{6-2} fractional factorial experiment design was implemented to enable an efficient study of this relatively large number of factors and to obtain information on the effects from their interactions. An early selection of AFM measurements has now identified features having CDs at the 20 nm level. The uniformity of individual reference-feature CDs exceeds those of the earlier delivery. It is thus anticipated that the uncertainties that will be ascribed to them at the completion of the experiment in FY2006 will be below the ± 1.5 nm to ± 3 nm range of prior deliveries in FY2005.

■ In preparation for implementing the findings of the process-optimization exercise referenced in the previous paragraph, and responding to the customer needs described earlier, chip layouts have been designed for three new SCCDRM fabrication ventures. Two of them are for 200 mm-wafer monolithic implementations. The first of these is an exercise to evaluate some available 200 mm (110) material, which is difficult to obtain but which we have on hand, for the wafer lots to be run on the 193 nm lithography tool at SEMATECH. The evaluation lithography is being accomplished with an i-line tool at the University of Edinburgh. The second is a design that is being incorporated onto a new reticle for lithography by the 193 nm Step-and-Scan tool on line in SEMATECH. The project drafted and delivered a comprehensive business plan for SEMATECH to use in communicating the scope of this venture to member companies and other potential external clients. The third venture for which new CAD has been designed is a new complex optical/e-beam-direct-write process, which is being applied to 100 mm (110) starting material. The lithographic processing for which the CAD has been designed will be carried out jointly by the Microelectronics Research Center, of the University of Texas at Austin, and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh.

One of the main drivers of the customers' need to replace the carrier wafer with a monolithic implementation is that the former is vulnerable to contamination originating during post-assembly cleaning. Ordinarily this is not a leading concern in AFM-tip calibration, although it cannot be dismissed for SCCDRM use in ultra-clean facilities. Otherwise, tip calibration is an application for which the reference materials are well suited and are becoming widely recognized. However, an emerging application of interest in the industry is SEM tool calibration. In this application, regular reference material cleaning is very necessary due to the nature of the metrology. During the current year, a new cleaning procedure was devised and evaluated at the chip level. At the same time, the rate of hydrocarbon deposition during worst-case conditions was assessed. This work was done to deal with the expected questions on the subject when the 200 mm wafer based artifacts become available.

- During the investigations of hydrocarbon contamination by SEM tools, and devising the cleaning procedure to deal with it, we took the opportunity to look at the issue of reference material calibration using HRTEM as the primary metrology and SEM as the transfer metrology. The attractiveness of this approach to calibration is that SEM is a much more readily available facility and is generally faster than AFM even though one can expect uncertainty inflation. The results were technically useful and have been incorporated into a manuscript that has been submitted to an IEEE Transactions journal.

- The emerging metrology known as optical-CD (OCD) scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes and AFMs require a vacuum wafer environment, OCD metrology does not and is fast and non-invasive. The possibilities of OCD extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of OCD control scatterometry may not be met. Since the SCCDRM implementation is well suited to the fabrication of calibrated reference materials for this new application, we have now accomplished the first-ever fabrication and inspection of gratings suitable for this purpose.

Recently, the project published a full-length report on the fabrication and calibration of a selection of SCCDRM Reference Materials entitled "Report of Investigation of RM 8111: Single-Crystal Critical Dimension Prototype Reference Materials." Editors of the NIST Journal of Scientific Research have invited, and have been provided with, a version appropriate for publication in that journal later this year. Several other papers on special aspects of the fabrication and calibration, such as test-chip design, AFM metrology, and HRTEM imaging, have been presented at the SPIE Spring Symposium of February, 2006, and the IEEE International Conference on Microelectronic Test Structures in March, 2006. A paper on the subject of etch-process optimization for uncertainty management has been accepted for presentation at the International Electron, Ion, and Photon Beam Technology and Nanofabrication Conference in June, 2006. A manuscript on the comparison of SEM-CD measurements and traceable-AFM CD measurements has been written and submitted to an IEEE Transactions journal.

Collaborations

The project is now actively collaborating with the Microelectronics Research Center of the University of Texas at Austin (http://www.mrc.utexas.edu/amrc/publications.html), and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh in Scotland (http://www.see.ed.ac.uk/IMNS/). Both these organizations have in operation the advanced wafer processing tools that we will be using to address the customer needs referenced in the sections above. Both institutions have highly skilled staff with both of which we have published recently. We are interacting with the CAD and reticle people the ISMI Subsidiary of SEMATECH, (http://ismi.sematech.org/) who have invited us to share space on a new reticle for their SVGL 193 nm Step-and-Scan lithography tool to fabricate an advanced generation of SCCDRMs for distribution to the member companies, as well as for possible calibration and distribution from NIST as SRMs.

We also interact regularly and closely with NIST's MEL and ITL Laboratories (http://www.mel.nist.gov/ and http://www.itl.nist.gov/) with both of whom we of EEEL share an intramural ATP program award to reduce the certified CDs and uncertainties of SCCDRMs through fabrication refinements.

Standards Committee Participation

Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

Recent Publications

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, "Implementation of Simulation Program for Modeling the Effective Resistivity of Nanometer Scale Film and Line Interconnects," NISTIR 7234, February, 2006.

JEDEC Standard JESD202, "Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress," March 2006. (Written by H. A. Schafft).

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, "Resistivity of Nanometer-Scale Films and Interconnects: Model and Simulation," 2005 IEEE International Integrated Reliability Workshop Final Report, pp. 139-140 (open poster). IEEE Catalog Number 05TH8799. ISBM 0-7803-8992-1. Library of Congress Number 2005920974.

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M. W. Cresswell, R. G. Dixson, W. F. Guthrie, R. A. Allen, C. E. Murabito, B. Park, J. V. Martinez de Pinillos, and A. Hunt "CD Reference Features with Sub-Five Nanometer Uncertainty" published in SPIE Proceedings Vol. 5752 (2005).

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, "Modeling and Simulation of Resistivity of Nanometer Scale Copper," Microelectronics Reliability. In-press. On-line publication date: December 19, 2005.

R. A. Allen, R. I. Patel, M. W. Cresswell, C. E. Murabito, B. Park, M. D. Edelstein, L. W. Linholm, "Recent Developments in Producing Test-structures for Use as Critical Dimension Reference Materials," ICMTS IEEE International Conference on Microelectronic Test Structures, Mar. 22-25, 2004, Awaji, Japan, pp. 35-40 (01-MAR-2004).

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H. A. Schafft, J. R. Lloyd, "Electromigration Discussion Group Summary," 2002 IEEE International Integrated Reliability Workshop Report, 2002 IEEE International Integrated Reliability Workshop, Oct. 21-24, 2002, Lake Tahoe, California, pp. 204-206 (01-FEB-2003).

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Optical-Based Photomask Dimensional Metrology

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T. Doiron

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay errors on the wafer and accurately measuring image placement of features on the photomasks. Overlay control is listed in multiple sections of Table 116 of the 2005 SIA ITRS as a difficult challenge for <32 nm processes. Overlay metrology and photomask feature placement metrology have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table 119a shows that there are current image placement and overlay control challenges with no known solutions for photomask image placement metrology beyond the 65 nm node. As shown in Table 119b, the problems are more acute for long term photomask CD metrology where the industry will soon be encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are two main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties.

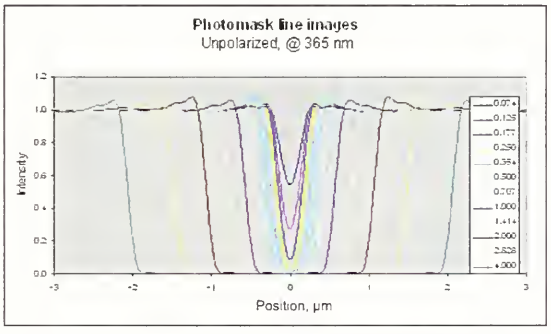

Figure 1. Modeling results for linewidth photomask samples showing CDs down to 0.25 µm.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 µm to 30 µm have been certified on the previous NIST green light optical calibration system. Linewidth uncertainties have been reduced to 20 nm, k=2. The next generation in this line of standards is SRM 2059 (Fig. 2, page 50), printed on a standard size 1.4×10^{-4} cm^3 substrate with calibrated linewidths and space-widths ranging from nominally 0.25 µm to 32 µm, and pitch patterns from 0.5 µm to 250 µm.

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology

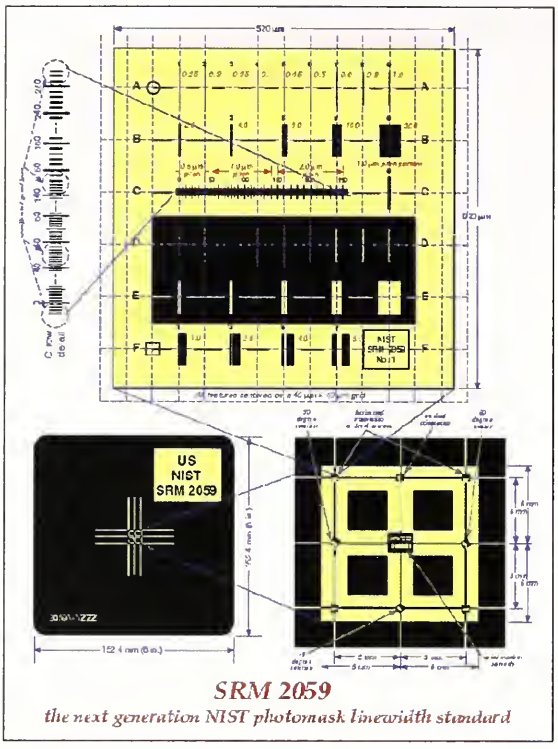

Figure 2. The new linewidth photomask standard.

through modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes.

DELIVERABLES:

- Compare and improve the accuracy of the NIST optical scattering code with new scattering models developed by Spectel and Panoramic Technologies for use in transmission. 2Q 2006
- Complete the second round of calibrations of SRM 2059 and complete the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 4Q 2005

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is now available as a NIST Standard Reference Material, # 5001. The artifact can be used by the semiconductor industry to standardize 2-D measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements.

A new generation of grid for the SRMs has been fabricated and another round of measurements is in process. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on the new Nikon 5i two-dimensional metrology tool at NIST. The Nikon 5i has been fully characterized and is now a calibration tool for grid calibrations. In response to industry needs, this tool is now under development for use as a wafer calibration tool for large distance position-to-position wafer calibration.

To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES:

- Develop a new set of comparator algorithms to enable the SRM 5001 calibrations to be completed with the Nikon 5i tool in collaboration with the industry Ipro system. Complete the comprehensive analysis capabilities for centerline and edge detection methods with a complete uncertainty statement. 2Q 2006
- Implement the standard scale correction and new mapping software for the Nikon 5I system. Measure the new set of two-dimensional calibration grids with a complete uncertainty. 1Q 2006
- Complete the second round of calibrations of SRM 5001 and complete the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 2Q 2006

Accomplishments

■ SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock has been sold.

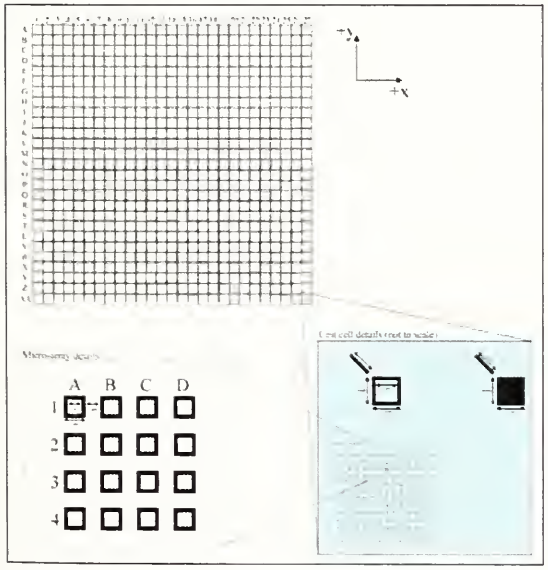

Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

■ NIST currently has completed the uncertainty analysis and documentation for *SRM 2059 Photomask Linewidth Standard*, which will enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks. The SRM 2059 photomask linewidth standard has been delivered and completed and is now for sale in the SRM office. This represents the only calibrated SRM linewidth standard currently available from NIST.

■ The first set of two-dimensional grid artifacts, known as SRM 5001, delivered to the SRM office and is selling well. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. A second set of re-designed 6-inch feature placement standards has now been measured and fully calibrated in the close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements and all documentation has been delivered to the SRM office and the second set of calibrated photomask grids will now be made available as a calibrated SRM.

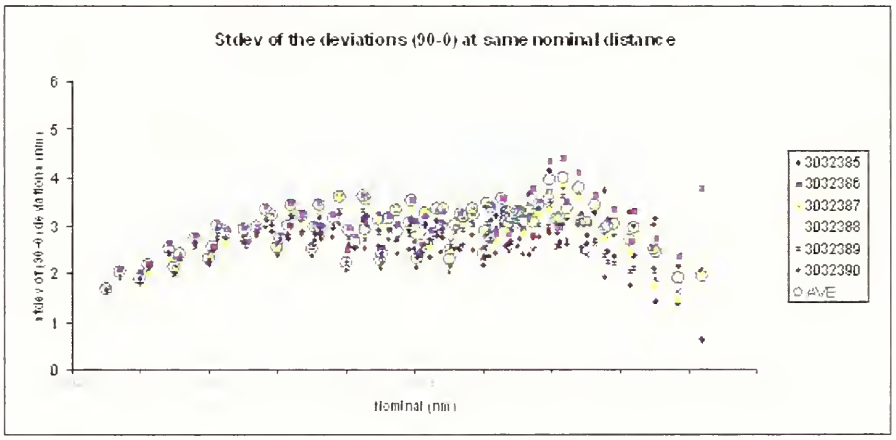

Figure 4 shows tool repeatability and mapping data for the two-dimensional mask calibration procedure.

■ In close collaboration with SEMATECH, we have completed a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection. This document is available through SEMATECH as a tech transfer document.

■ A comprehensive suite of two dimensional calibration methods for the calibration of optical systems and illumination systems is being

developed based on the SRM 5001 grid calibration methodology. Some of these results were recently published at SPIE Microlithography. These methods are enabling a substantially improved optical calibration and alignment sequence as well as improved modeling inputs for more accurate linewidth measurements.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

Recent Publications

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J. Potzick, "The Neolithography Consortium," *Proceedings of SPIE 25th International Symposium on Microlithography*, vol. 3998-54 (2000).

M. Schroeck, and T. Doiron, *"Probing of two-dimensional grid patterns by means of camera based image processing,"* accepted by SPIE for January 2000.

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Model-Based Linewidth Metrology

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth and line edge roughness metrology with uncertainties at the order of 1 nm level required by the industry roadmap.

Customer Needs

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, with projected worldwide sales of $254.7 billion in 2006 [Reuters, April 7 2006, reporting on iSuppli forecast]. As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 65 nm technology node."

To support present and future semiconductor technologies, industry needs to measure gate electrode widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 3 nm and with measurement precision (3 standard deviation repeatability) better than 0.6 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth *variation*, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2005 ITRS specifies that LWR, measured as three standard deviations of the CD, must be less than 2 nm in 2007 and be measured with better than 0.4 nm precision.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices. Barriers to accurate LWR measurement include random errors due to noise or sampling and poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness").

Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have developed a model-based library method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories. This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is

Technical Contact:
J. Villarrubia

"Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2005).

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline."

International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2005).

likely to encounter in a measurement. The resulting actual shape/calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match (Fig. 1). The corresponding line shape is assigned to the unknown. In practice there may be more than two parameters, and the library may be interpolated.

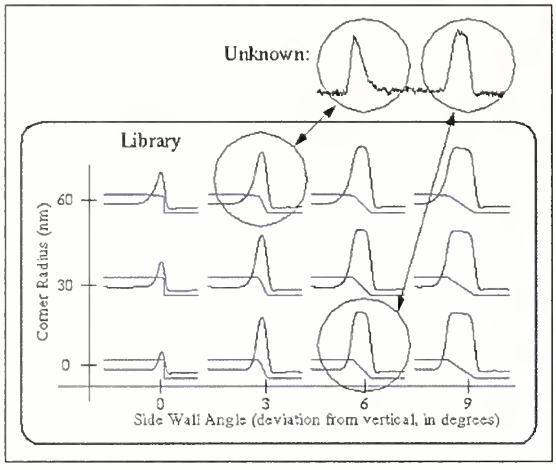

Figure 1. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

In recent years we have reported encouraging results for this method. Results for polycrystalline Si are shown in Fig. 2a and Fig. 2b. Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fabricated in Si rather than resist because resist geometry is too unstable for a long-term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination, charging, and shrinkage when imaging nonconducting resists may result in poorer accuracy for resist samples than for Si samples. Results for a UV resist are shown in Fig. 2c.

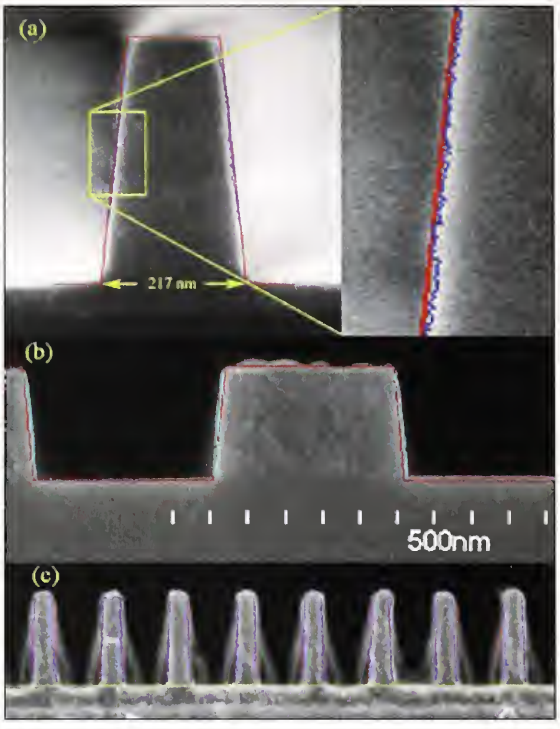

Figure 2. Agreement between MBL and cross-section measurements (a) for isolated polycrystalline ("poly") Si lines in which top-down measurements were performed with a laboratory SEM, (b) for dense poly lines measured with a commercial CD-SEM, and (c) for dense UV resist lines measured with a commercial CD-SEM. In all cases the red lines are the cross sections predicted by the MBL technique based upon top-down measurements, and the blue lines are edges assigned based upon the cross sections.

In 2006, we are improving the capabilities of the underlying modeling tools used to generate libraries. The existing simulation codes are limited to certain classes of sample shapes, essentially lines uniform along their length and with cross sections characterized by a small number of geometrical parameters, *e.g.*, width, sidewall angle, and corner radius. Improvements to the modeling code would permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, and line footing. We are also encouraging further adoption of this method by CD-SEM suppliers by further publication of the method, by making modeling software freely available to CD-SEM manufacturers, and by collaboration with their engineers.

DELIVERABLES:

- Make a detailed plan for how to handle 3-dimensional geometrical descriptions for SEM modeling. Write software that implements and test the description. 3Q 2006

- Write a software module that implements scattering physics. Merge scattering code and geometrical code into a simulation code for 3-dimensional samples. 4Q 2006

With regard to LWR measurement issues, last year we published a means of estimating LWR that measures and corrects for the false noise component of roughness. The result is an unbiased estimate of LWR (Fig. 3). However, in the limit when actual roughness is comparable to or smaller than the noise roughness term, random measurement errors can cause the correction term to sometimes be over-estimated, with the result that the estimated R^2 is negative. We are currently investigating Bayesian roughness estimators that do not have this undesirable property.

DELIVERABLES: Derive a Bayesian probability distribution function for linewidth roughness variance given a set of measurements. Use the function to determine reasonable estimates of LWR and uncertainty. Submit the results to an appropriate journal or conference proceedings. 3Q 2005

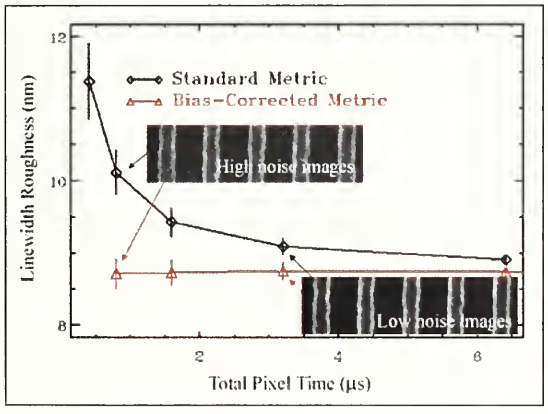

Figure 3. Measured LWR vs. pixel integration time for two different LWR metrics. Lower pixel integration time corresponds to higher noise in the image. Vertical bars are ±1 standard deviation of the observed repeatability. These were repeated measurements at the same location—therefore all measured values ought to be the same and any observed dependence of LWR upon pixel integration time must be a measurement artifact.

Accomplishments

- We have improved our understanding of several physical processes, including work function barrier penetration by electrons, electron transport through dilute gases (relevant to the use of variable pressure SEM, proposed for mask metrology), and the effect of target electron binding energy upon scattering cross sections. This work is in preparation for including this improved physics in future models of SEM performance.

- We showed that NIST's model-based library metrology method is less sensitive to SEM misfocus than standard methods. There nevertheless was some measurable sensitivity, which we attributed to breakdown of our beam shape model at large defocus. This indicates a need for future model software to include more accurate beam shape information.

- We were awarded a Dept. of Commerce Silver Medal and a Nano50 2005 Technology Award, for the model-based library technique, one of the "top 50 innovators, techniques, and products impacting the commercialization of nanotechnology to mainstream markets."

- We completed work on an unbiased linewidth roughness estimator and published the results in Proceedings of the SPIE Microlithography conference. This publication was awarded the Diana Nyyssonen "Metrology Best Paper of 2005" award by conference organizers.

Collaborations

International SEMATECH, Benjamin Bunday, Michael Bishop.

Hitachi, Ltd., Maki Tanaka.

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Atom-Based Dimensional Metrology

Technical Contact:
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable and allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

Customer Needs

This project responds to the U.S. industry need for length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer tremendous promise for meeting these future measurement, test artifact, and calibration standards needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a unique NIST-designed picometer resolution interferometer (Fig. 1).

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of linewidth metrology tools. We are also developing unique high-resolution interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions at the nanometer scale. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

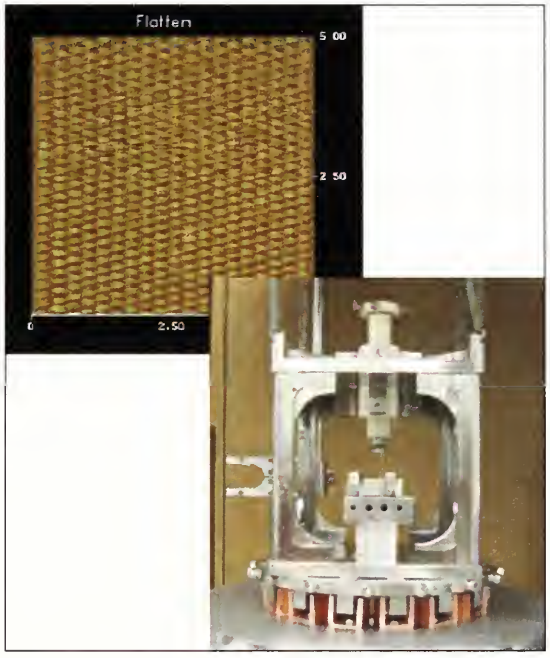

Figure 1. A new STM structure design has been implemented to improve the atomic scale imaging and structural characteristics. This system will provide improved nanometer scale interferometer-based imaging and measurement capabilities.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (Fig. 2, page 58).

As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of having samples

of known geometry and width essential. This project is developing samples of known geometry and atomic surface structure which yield well defined dimensional measurements. One goal is a measurement which results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (Fig. 3).

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods

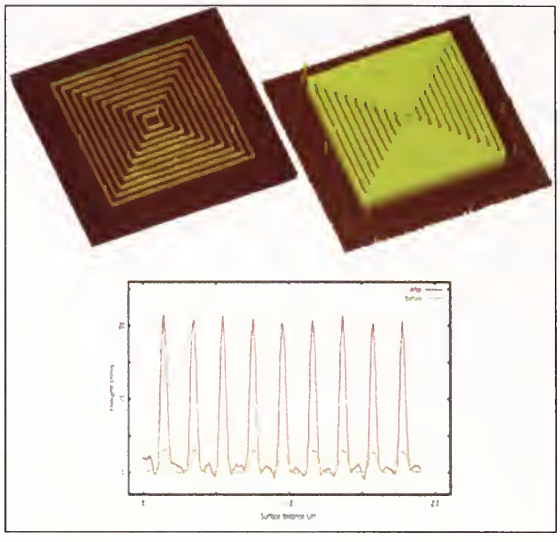

Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

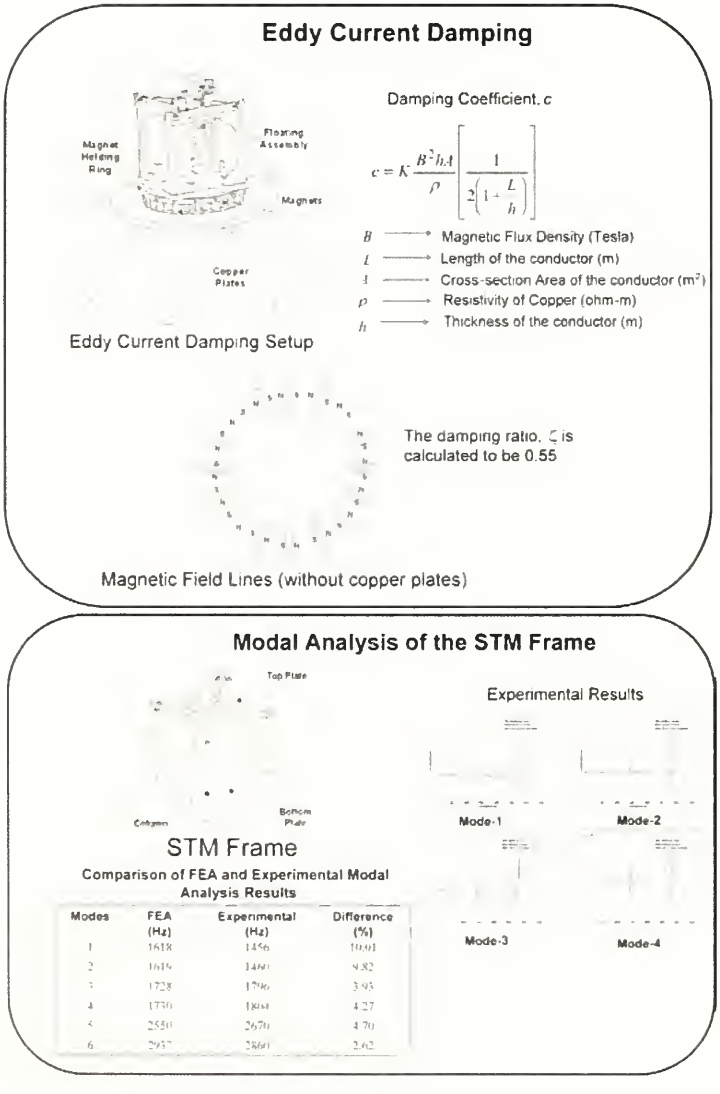

Figure 2. Key design elements for the instrument used to fabricate features with sub-10 nm dimensions. This tool utilizes advanced design tools to optimize vibration sensitivity and enable access to 1 cm x 1 cm of sample area.

that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order which is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES:

- Write features in silicon with critical dimensions smaller than 10 nm. Apply the pattern writing process and etch features for use as optical scatterfield test structures using the new STM.
  3Q 2006
- Work with EEEL and ISMT to develop improved methods for etching nanostructures written in silicon. Use RIE etching techniques to etch features with sub-10 nm dimensions in silicon.
  4Q 2006

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These

well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Investigate altemative W tip crystalline structures and high temperature preparation methods for use in high resolution imaging. Determine the stability of these W tips for use as STM imaging and fabrication tips. 3Q 2006

3. Focus on the development of artifacts that can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and have also demonstrated atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing *in-situ* processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures (Fig. 4).

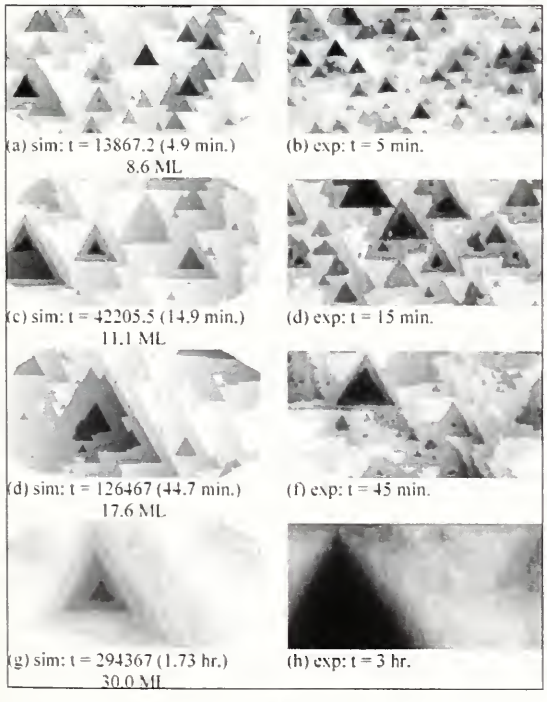
(a) sim: t = 13867.2 (4.9 min.)
8.6 ML
(b) exp: t = 5 min.
(c) sim: t = 42205.5 (14.9 min.)
11.1 ML
(d) exp: t = 15 min.
(d) sim: t = 126467 (44.7 min.)
17.6 ML
(f) exp: t = 45 min.
(g) sim: t = 294367 (1.73 hr.)
30.0 ML
(h) exp: t = 3 hr.

Figure 4. Time resolved KMC simulation for surfaces with 0.02° miscut angle and 60° miscut orientation on the left and compared with experimental data on the right. All images are 4000 × 2000 nm².

DELIVERABLES: A new STM which has improved atomic scale imaging capability for atom-based dimensional metrology is now operational. We are implementing a UHV sample and tip heating and preparation capability which interfaces with the system transfer mechanism for sample transfer into the UHV environment. The new STM and UHV preparation facility will allow improved Si sample prep and atomic surface reconstructions. 4Q 2006

4. Develop and publish on the objective for *in-situ* stabilized, atomically ordered surfaces that can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples require extensive surface preparation and modeling to achieve repeatable Si surfaces for metrology and fabrication purposes.

Accomplishments

- We have prepared atomically flat surfaces and obtained atomic order on the wet chemical prepared surfaces. The routine imaging of these surfaces on the atomic scale should be enhanced with the new STM currently being implemented. These results have been recently published in leading chemical physics journals and presentation forums. These results are a substantial step forward in repeatable silicon surface preparation for atomic scale metrology and are now being supported in collaboration with SEMATECH and current industry requirements.

The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been published as an archived journal article. We are now implementing a robust and repeatable tip processing capability in both UHV STM systems.

- Develop the advanced modeling requirements to fully simulate the new STM structure. We have completed finite element analysis (FEA) simulations which test the dynamic modes of the STM and interferometer structure. These results have

significantly improved the structural designs. Publications in the area of STM structural modeling and STM structural damping for improved dynamics have been instrumental in recent tool improvements and in enhancing our collaboration with the George Washington University.

The results, seen in Fig. 4, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

- The etching process has been developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A publication recently appeared on this material. The importance of etching structures in Si (111) is now being supported by SEMATECH and a recent collaboration between NIST and SEMATECH to develop lithography methods and plasma etch method at SEMATECH's fab is now underway.

- We have used the FIM techniques to analyze nanotubes and their structure. The nanotubes were directly characterized for use as SPM tips with dimensional analysis on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology (Fig. 5).

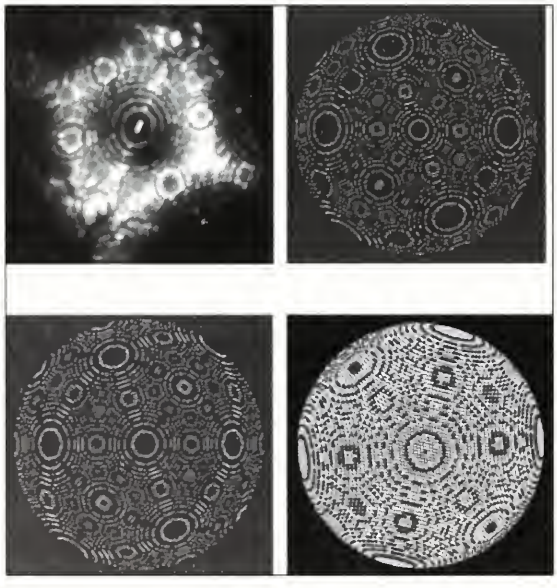

Figure 5. Upper left shows an FIM image of a W (110) tip. On the upper right is a simulation of a FIM image of a W (110) tip with base radius r = 14.9 nm and n = 1.82. The lower panels show simulations of an FIM image of a W (110) tip with base radius r = 14.9 nm and n = 2 and a ball model with same parameters.

- We have measured directly the surface atom spacings based on an interferometer measurement. We have fitted our UHV STM with a high accuracy sub angstrom resolution interferometer. We have closed the loop and made atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

- The results for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty have been published in Optical Engineering. These results were also presented at the ASPE conference and SPIE to make the new interferometry methods available to the industry.

Collaborations

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics., George Washington University.

Recent Publications

S. Chikkamaranahalli, R. Vallance, B. Damazo, and R. M. Silver, *"Damping Mechanisms for Precision Applications in UHV Environment,"* Proc. ASPE Conf., Pitts. PA (2006).

H. Zhou, J. Fu, and R. M. Silver, *"A Time-resolved Kinetic Monte-carlo Simulation Study on Si (111) Etching,"* Submitted to Journal of Physical Chemistry (2006).

S. Chikkamaranahalli, R. Vallance, B. Damazo, R. M. Silver, and J. Gilsinn, *"Dynamic Modeling and Vibration Analysis of a UHV Scanning Tunneling Microscope,"* Proc. ASPE Conf., Norfolk VA (Oct. 2005).

H. Zhou J. Fu, and R. M. Silver *"The Influence of Defects on the Morphology of Si (111) Etched in NH_4F,"* J Chemical Physics B. 109, 23386 (2005).

J. Gilsinn, H. Zhou, B. Damazo, J. Fu, R. Silver, *"Nano-Lithography in Ultra-High Vacuum (UHV) for Real World Applications,"* Proc. NanoTech (2004).

J. A. Dagata, C.A. Richter, R.M. Silver, E. Vogel, J.V. Martinez de Pinillos, *"Metrology Development for the Nanoelectronics Industry at the National Institute of Standards and Technology,"* Proc. NanoTech (2004).

H. Zhou, *"Study of wet chemically prepared hydrogen terminated Si (111) surfaces and a novel implementation of a high resolution interferometer,"* Thesis, University of Maryland, 2004.

R. M. Silver, S. Gonda, J. Jun, L. Howard, and C. Jensen, *"Atomic Resolution Measurements with a New Tunable Diode Laser-Based Interferometer,"* Optical Engineering, Vol. 43 No. 1 (Jan. 2004).

P. V. M. Rao, C. P. Jensen, and R. M. Silver *"An enhanced model for STM tip geometry measured with FIM,"* JVST B (Mar/Apr 2004).

Wafer-Level and Overlay Metrology

Technical Contacts:
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T. Doiron

Goals

Provide technological leadership to semiconductor and equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high throughput, lower cost of ownership metrology tools, which enable more dense sampling strategies has lead to a comprehensive program at NIST to both support and advance the optical techniques needed to make these overlay and photomask/wafer critical dimension measurements (see Fig. 1).

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in multiple sections of Table 116 of the 2005 ITRS as a difficult challenge for both >32 nm and <32 nm processes. Overlay measurements have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table 118a shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 118b, the problems are more acute for long term CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are two main strategic technical components of this project.

1. NIST has developed an overlay metrology tool that has undergone continuous development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. The technical strategy for overlay metrology is divided into two segments: (a) instrumentation development and the advance of overlay metrology techniques, and (b) the design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will

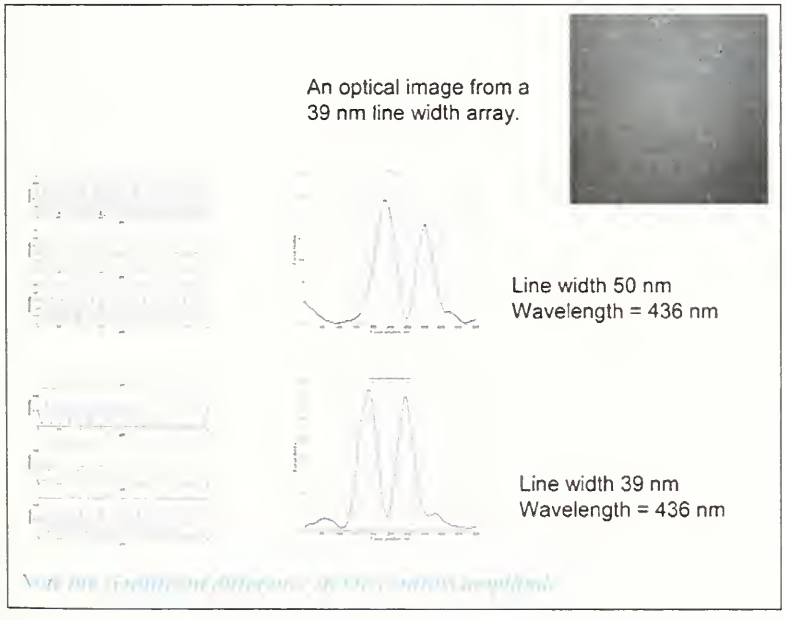

Figure 1. The image is a CCD camera image from an array of 39 nm CD features etched in polysilicon. The panels in the center column each show sets of profiles from the peaks and valleys of the through-focus focus metric curves, seen on the right. The upper two panels are from 50 nm CD linewidth arrays while the lower two are from the 39 nm linewidth array. These data were acquired with 0.4 illumination NA, 0.8 collection NA, and 436 nm wavelength.

translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS) (Fig. 2).

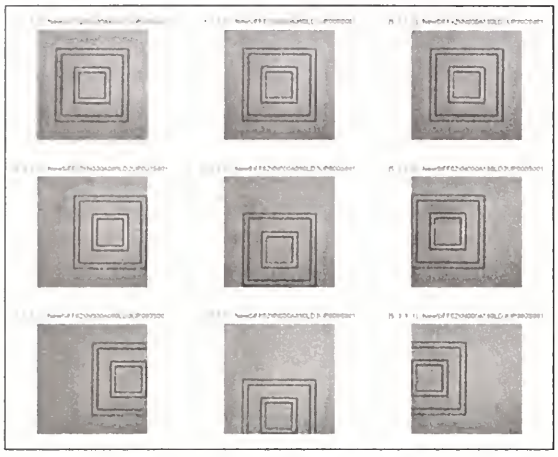

Figure 2. An example of reversal methods applied to determine WIS and the asymmetry of the target itself.

A set of standard artifacts and procedures, developed at NIST and published, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement system used for this component is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high resolution image capture with a full field CCD data acquisition system which has been fully characterized and calibrated. This instrument has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems have been evaluated and improved edge detection and CCD array calibration procedures have been implemented. These same methods for two-dimensional CCD array analysis are now being applied to optical component alignment error and aberration analysis.

Standard overlay artifacts have been fabricated in 200 mm and 300 mm wafers and calibrated for SRM distribution. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for example, Fig. 3.

We have also developed a series of new overlay targets and linewidth targets intended to enable the measurement of overlay and linewidth with device

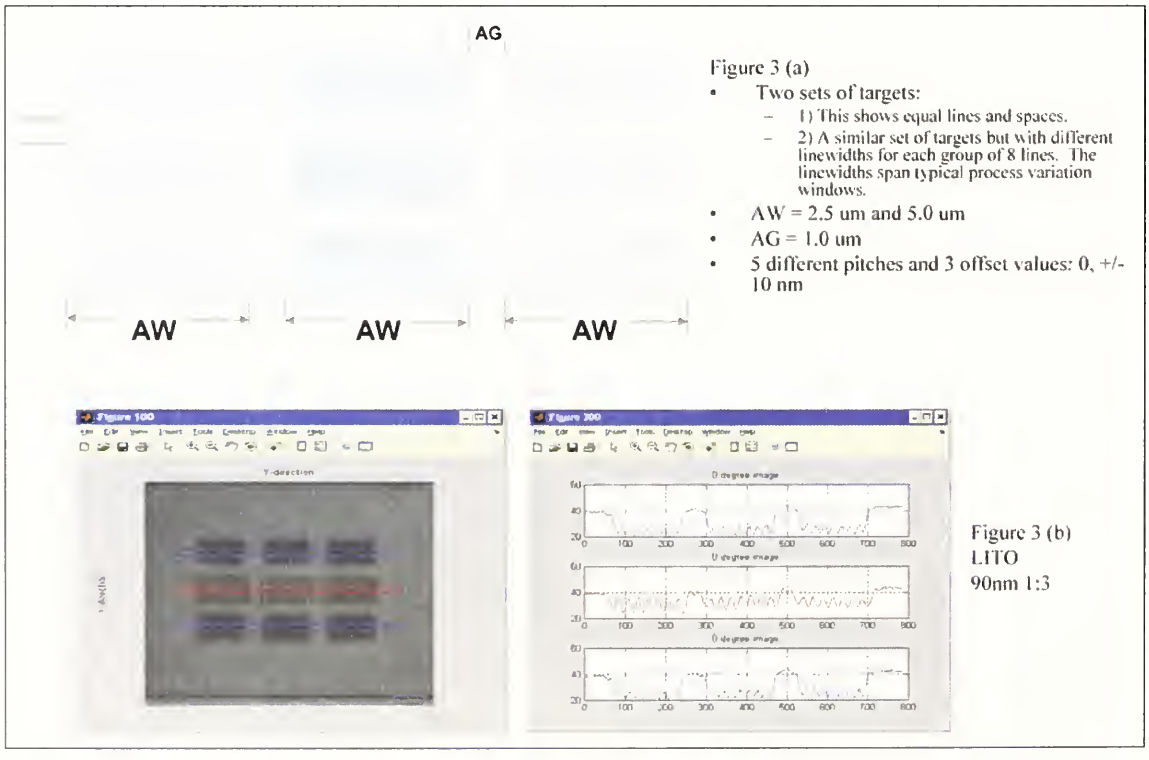
AG
Figure 3 (a)
• Two sets of targets:
– 1) This shows equal lines and spaces.
– 2) A similar set of targets but with different linewidths for each group of 8 lines. The linewidths span typical process variation windows.
• AW = 2.5 um and 5.0 um
• AG = 1.0 um
• 5 different pitches and 3 offset values: 0, +/- 10 nm
AW
AW
AW
Figure 3 (b)
LITO
90nm 1:3

Figure 3. A schematic of the target designs is shown in (a). This is one example of several variations of this design. The lower part of the figure shows an image and a set of profiles for a target which reflects higher-order optical content.

sized features. A variation of these targets allows in-chip targets to be placed throughout the active area of a die. These results have been published recently and collaborative work is progressing to develop the commercial applications to measure overlay using device sized features in targets of small overall dimension. There is also a comprehensive effort developing new high resolution overlay targets intended to enable the continued use of optical overlay measurements for the 65 nm node and beyond. An example of the latest high resolution targets is shown in Fig. 4.

DELIVERABLES:

- Publish an improved set of alignment and characterization tests for the overlay microscope, optics, and the *x-y* metrology stage. Use these new qualification techniques in the final uncertainties and tabulated combined uncertainty values for the latest set of SRM calibrations. This includes the characterization and calibration of complex optical alignment effects on overlay output values. 2Q 2006
- Use the OMAG 4 metrology reticles from the SEMATECH collaboration to fabricate a new set of overlay calibration targets/wafers. Work with SEMATECH and the Overlay Metrology Advisory Group (OMAG) to develop and publish a new set of calibration techniques verified for calibration of industry tools. This includes measurement protocols for evaluating wafer induced shift (WIS) and asymmetry components from the wafer. 2Q 2006
- Work with SEMI and SEMATECH in the development of new target designs and standards specifications for overlay metrology. This new specification is focused on bringing some standardization back to the overlay target designs and a move away from the growing number of proprietary overlay target designs, for calibration purposes. 4Q 2006

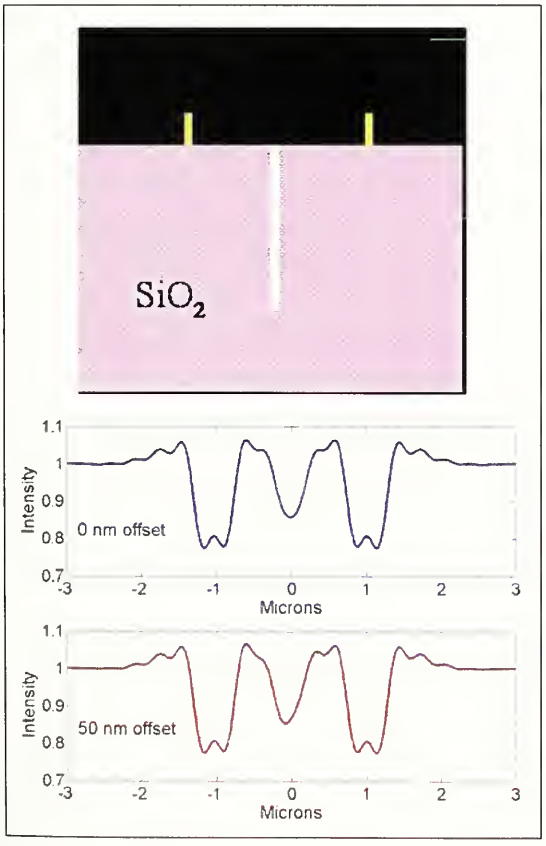

Figure 4. New proposed overlay targets which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

Modeling the effects of all of the relevant feature properties encountered in overlay measurements and optical critical dimension measurements using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 5. NIST has a world class effort in optical modeling. This includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and the NIST-developed exact integral equation solver method. The latter method has become recognized as the most accurate in existence today.

DELIVERABLES:

- Compare and test the accuracy of new scattering models for line width evaluation in reflection mode and transmission mode. Develop a standard set of simulation values and make them available for comparison and verification by industry users. 3Q 2006

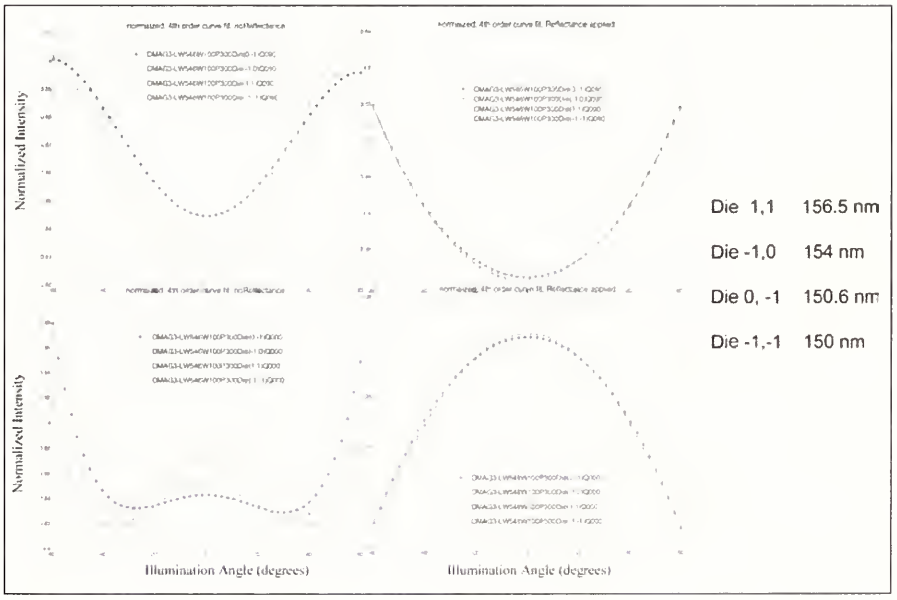

Figure 5. TM polarization is on top and TE is shown on the right. The vertical axes are units of normalized intensity and the horizontal axes are illumination angle in degrees. The data show good sensitivity to nm changes in linewidth. The image has been normalized to the background. A fourth order fit is used to analyze the data. The dynamic range is in part the result of the background normalization.

- Develop new calculation methods for analyzing asymmetric overlay targets. Compare with modeling results of more standard double-etched silicon structures. 1Q 2006

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This methodology has demonstrated the possibility of using optical methods for line width and overlay metrology with targets composed of features smaller than 50 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is well suited for high resolution microscopy of metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods which can be suitably applied to device-sized features. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are showing promise as potential solutions to these significant metrology challenges. As a part of this project, we have developed a new optical tool specifically intended to make this type of scatterfield measurement. This effort includes comprehensive optics modeling as well as a new optical configuration designed in-house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

DELIVERABLES:

- Develop a comprehensive set of techniques to accurately measure optical illumination fields and publish results. Develop similar characterization methods to measure the collection optics set of aberrations and to perform optimum optical alignment. 2Q 2006
- Develop fully automated focus and positioning control systems for the new scatterfield microscope. Complete the optical component design and layout for the new tool and assemble the illumination optics in an open architecture configuration. Test the new optical tool to verify performance using scatterfield optical techniques. 4Q 2006

Accomplishments

■ Researchers from the overlay metrology project have submitted a CD 240 for the disclosure of recent potential breakthrough material in high resolution optical metrology. As a part of this disclosure, a new method was proposed and subsequently verified in the laboratory. This new approach is capable of measuring features at least as small as 20 nm in dimension with densities to one to one line/space ratio.

■ NIST electromagnetic scattering code: Further successful applications of the NIST electromagnetic scattering code developed by E. Marx and two other industry codes have resulted in detailed comparisons and study of arrayed targets. These model extensions are providing simulations results and guidance in optical tool design and metrology target designs for features currently down to 50 nm. The models are now capable of simulating targets in array formats as well as illumination at a single angle for analysis and development of scatterfield methods.

■ High resolution scatterfield optics successful: The optics project which was successful as champion for the Scatterfield competence proposal has proved to be very productive. The cross laboratory proposal has produced several recent results which were published and presented at the recent SPIE Microlithography meeting. The collaboration between the Manufacturing Engineering (MEL) and Physics (PL) laboratories has published results this year on the evaluation and results of high resolution optical methods involving scatterometry and the new scatterfield methods being developed within Precision Engineering Division (PED). The work also involves technical evaluation of the key issues associated with optical modeling and the n and k input parameters.

■ Significant industry interest in new high-resolution optical methods being developed under the Scatterfield Microscopy title. Following invited presentations at SEMATECH OMAG and Advanced Metrology Advisory Group (AMAG) metrology workshops, and discussions at SPIE, there was much interest in the surprising results of 40 nm sized features. These results obtained by optical methods are some of the smallest features shown to these audiences and go well beyond the expected capabilities of these tools.

■ NIST researchers have made model comparisons between the E. Marx developed optical scattering code, the Spectel company Metrologia metrology modeling package, a recently NIST developed code by T. Germer and the Panaramic Technologies FDTD code. Different material systems were compared as well as detailed mate-

rial comparisons some of which were published recently. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement based on recent code enhancements and improvements. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results have been presented at SPIE Microlithography.

- New scatterfield optical tool operational. The new scatterfield metrology tool has been assembled and is now operational in the Advanced Metrology Laboratories. This tool is specifically designed for performing sophisticated illumination engineering and scanning and has already produced important results. The new tool is fully computer controlled and based on a NIST designed optical column to enable access to a large conjugate back focal plane for illumination engineering. The new tool has been instrumental in investigating recent uncovered polarization dependent transmission effects in the optical train.

- Reflection mode optical measurements of phase shifting photomasks. The first round of measurements and model comparisons between profiles from phase shifting reticles has been completed. These results obtained in reflection mode have compared experimental measurements with modeling results obtained using the Egon Marx electromagnetic scattering code. These results were documented and summarized in a SEMATECH final report.

- The NIST Overlay Metrology project leader has played a significant role in the (OMAG) of SEMATECH. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers and tool suppliers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project, in particular, the recently published methods for evaluating in-chip and device sized overlay targets. In addition, CCD array performance and overall optical system characterization and calibration performance measures developed at NIST have been adopted.

- Members of the optical metrology project met with several leading optical metrology tool manufacturers and international measurement laboratories regarding recent advances in the scatterfield microscopy technique. The individual discussions included details about the new high resolution microscopy techniques being developed at NIST and their potential industrial application and implementation. Research in the area of high resolution optical methods is now being pursued at several companies with clear applications in overlay metrology and potential applications in optical based critical dimension metrology. The discussions largely focused on potential technology transfer between the NIST optical projects and development scientists at the optical metrology companies. Details on recent techniques for optical aberration measurements and on methods for evaluating Kohler illumination were covered.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

Recent Publications

R. M. Silver, B. Barnes, R. Attota, J. Jun, J. Filliben, J. Soto, M. Stocker, P. Lipscomb, E. Marx, H. Patrick, R. Dixson, and R. Larrabee, *"The Limits of Image-based Optical Metrology,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520Z (2006).

R . Attota, R. M. Silver, M. Bishop and R. Dixson, *"Optical Critical Dimension Measurement and Illumination Analysis using the Through-focus Focus-metric,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520K (2006).

Y. J. Sohn, B. Barnes, L. Howard, R. Silver, R. Attota, and M. Stocker, *"Kohler Illumination in High Resolution Optical Metrology,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61523S (2006).

H. Patrick, R. Attota, B. Barnes, T. Germer, M. Stocker, R. M. Silver, and M. Bishop *"Scatterfield Microscopy using back focal plane imaging with an engineered illumination field,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520J (2006).

P. Lipscomb, J. Allgair, B. Bunday, M. Bishop, R. Silver, R. Attota, and M. Stocker, *"Calibration Optical Overlay Measurements,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 615211 (2006).

D. Kandel, M. Adel, A. Frommer, V. Levinski, A. Rapoport, and R. M. Silver, *"Imaging Simulations of Optimized Overlay Marks with Deep Sub-resolution Features,"* Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61522X (2006).

R. M. Silver, R. Attota, M. Stocker, M. Bishop, L. Howard, M. Davidson, T. Germer, and R. Larrabee, *"High-resolution Optical Metrology,"* SPIE Vol. 5752, (2005).

R. Attota, R. M. Silver, T. Germer, M. Bishop, R. Larrabee, M. Stocker, L. Howard, *"Application of Through-focus Focus metric Analysis in High-resolution Optical Metrology,"* SPIE Vol. 5752 (2005).

R. M. Silver, R. Attota, M. Stocker, M. Bishop, J. Jun, E. Marx, M. Davidson, and R. Larrabee, *"High-resolution Optical Overlay Metrology,"* SPIE Vol. 5375 P. 78 (2004).

R. Attota, R. M. Silver, M. Bishop, E. Marx, J. Jun, M. Stocker, M. Davidson, R. Larrabee, *"Evalnation of new in-chip and arrayed line overlay target designs,"* SPIE Vol. 5375 P. 395 (2004).

J. M. Pedulla, J. Potzick, R. Silver, and R. Larrabee, *"Improving the Uncertainty of Photomask Linewidth Measnrements,"* SPIE Vol. 5375 P. 317 (2004).

Front-End Processing Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The gate dielectrics, traditionally SiO_2 and SiON, will soon no longer be viable. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and technology infrastructure to support the measurement of wafer thickness variation of 300 mm silicon wafers, and surface flatness of chucked wafers.

Customer Needs

Decreasing line-widths, the accompanying reduction in depth of focus, larger wafer diameters for current stepper lithography applications, and the advent of immersion lithography place ever increasing restrictions on wafer flatness and the required measurement uncertainty. The International Technology Roadmap for Semiconductors (ITRS) 2005 edition projects a site flatness of ≤ 45 nm in 2010 for DRAM contacted and MPU/ASIC Metal 1 ½ pitch of 45 nm, Front End Processes Section, Table 67a, page 7. We are focused on meeting customer requirements for calibrated thickness variation maps of free form wafers and flatness measurements of chucked wafers. We are addressing the need for standard 300 mm wafers with calibrated thickness variation with Improved Infrared Interferometer (IR^3) at NIST. These independent, traceable wafer thickness calibrations enable manufacturers of wafers and wafer metrology instruments to certify the performance of their metrology instruments. In addition, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometeR" (XCALIBIR). XCALIBIR has a 300 mm aperture for flat measurements and provides a way of verifying models of wafer/chuck interactions.

Technical Strategy

1. The IR^3 interferometer is an infrared phase-shifting interferometer, operating at a wavelength of 1550 nm which measures the thickness of low-doped silicon wafers up to 300 mm diameter in a single measurement (see Fig. 1a and Fig. 1b). The interferometer may be used in several configurations with collimated and spherical test wave-fronts. The collimated wave-front mode is the current focus of the project. In this method, the planar infrared wave-front is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wave-fronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation. Figure 2 (page 70) shows the thickness variation map for a 300 mm silicon wafer.

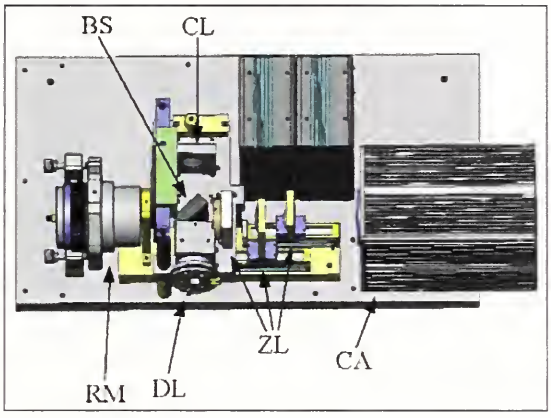

Figure 1a. NIST's infrared interferometer (IR^3). The main components of the interferometer are: collimator lens (CL), polarizing beam splitter (BS), phase-shifting reference mirror mount (RM), diverger lens (DL), zoom lens system (ZL), and camera (CA).

Figure 1b. Test end of the IR^3 setup for TTV measurements of 300 mm wafers. The picture shows the collimator lens together with a silicon wafer and a return flat.

DELIVERABLES:

- Install interferometer in clean-room for calibration measurements, 4Q 2005.
- Develop complete uncertainty analysis for thickness and thickness variation measurements. Ongoing
- Install laser with wide tuning range to enable measurements of very thin wafers. Ongoing

Technical Contacts:
U. Griesmann
R. Polvani

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer-chuck interaction studies are enabling advances in the state-of-the-art of wafer chucking that are essential to fully realize the potential of short wavelength lithography. WFSI's ability to collaborate with NIST in this area is critical to us."

T. D. Raymond
Wavefront Sciences, Inc., Albuquerque, NM

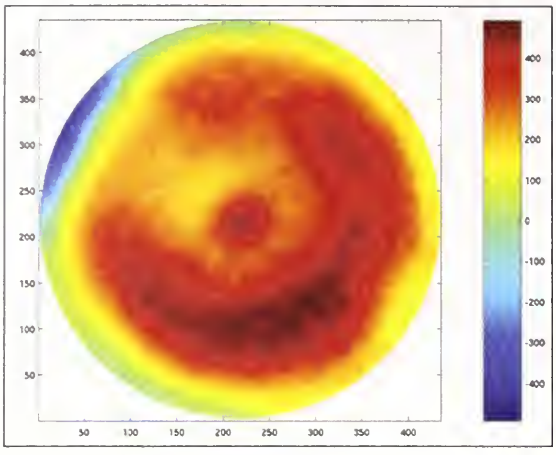

Figure 2. Thickness variation, with piston term subtracted, of a 300 mm double-side polished silicon wafer measured with IR³. The height unit is nm, the coordinates in x- and y-direction are detector pixel numbers.

2. A component in the evaluation of chucked wafer non-flatness is the characterization of interactions between the vacuum chuck and wafer. We are collaborating with Wavefront Sciences, Inc. (WFSI), Albuquerque, New Mexico and potentially one or more lithographic stepper manufacturers to help understand these interactions. WFSI is carrying out numerical analyses of the chuck/wafer interface for various chuck geometries. Figure 3 shows a model of XCALIBIR, a general purpose 300 mm aperture phase measuring interferometer developed at NIST, which is used to measure the flatness of chucked wafers. These can then be used to evaluate the influence of wafer/chuck interactions on the chucked wafer flatness.

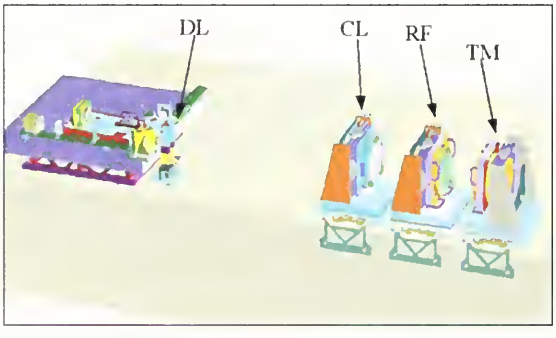

Figure 3. XCALIBIR interferometer configured for flatness measurements. The main components of the interferometer, from left to right, are: breadboard with source and imaging optics, diverger lens (DL), collimator lens (CL), reference flat (RF), and test mount (TM). For silicon wafer flatness measurements a wafer chuck is mounted on the test mount.

Accomplishments

- IR³ has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled to 2 pixels/mm. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty. In addition, a new laser with wide tuning range will make it possible to measure very thin wafers.

- The optical components in the IR³ interferometer were improved to reduce the measurement noise. Wavelength phase-shifting has been implemented and a TTV map repeatability of 5 nm peak to valley has been achieved for 300 mm wafers.

- The IR³ interferometer is being moved to a clean-room which will allow us to make calibration measurements of wafers supplied by industry customers.

- The flatness of 200 mm and 300 mm diameter wafers in the chucked condition was explored using the XCALIBIR interferometer.

Collaborations

During the course of this project, we have worked with several companies on problems relating to wafer flatness metrology and chucked wafer flatness.

1. WaveFront Sciences: Flatness measurements of free form and chucked wafers for metrology tool validation.
2. MEMC Electronic Materials: Wafer thickness standard development.
3. Siltronic: Wafer thickness standard development.
4. Intel: Development of very thin silicon thickness standards.
5. QED Technologies: Development of ultra-flat wafers.

Recent Publications

Q. Wang, U. Griesmann, and R. S. Polvani, "Interferometric Thickness Calibration of 300 mm Silicon Wafers" *Proceedings of the ASPE Topical Meeting on Precision Interferometric Metrology*, Middletown, CT (2005).

U. Griesmann, Q. Wang, and T. D. Raymond, "Optical Flatness Metrology for 300 mm Silicon Wafers," *AIP Proceedings of the 2005 Conference on Characterization and Metrology for ULSI Technology*, University of Texas, Richardson, TX, USA (2005).

D. R. Neal, P. Pulaski, T. D. Raymond, D. A. Neal, Q. Wang, and U. Griesmann, "Testing highly aberrated large optics with a Shack-Hartmann wavefront sensor," Proc. SPIE 5162, 129-138 (2003).

T. L. Schmitz, A. Davies, C. J. Evans, and R. E. Parks, "Silicon wafer thickness variation measurements using the National Institute of Standards and Technology infrared interferometer," *Opt. Eng.* **42**, 2281-90 (2003).

Modeling, Measurements, and Standards for Wafer Surface Inspection

Goals

Our goals are: (1) provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces; (2) develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS); and (3) investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, nonmetallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem currently exist for particles on bare silicon, on non-metallic films, and on wafer backsides, while it is anticipated that no acceptable solutions will exist for metallic films in 2010. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in-situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. It is anticipated that accurate calibration particles as small as 30 nm will be needed soon.

By 2010, at the 45 nm node, particles having diameters 22.5 nm must be detectable on bare silicon and nonmetallic films, with 36 nm on metallic films. No known solutions exist at this time. [2005 ITRS, Yield Enhancement, Table 113a]

Technical Strategy

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvements in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for

Technical Contact:
T. A. Germer

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

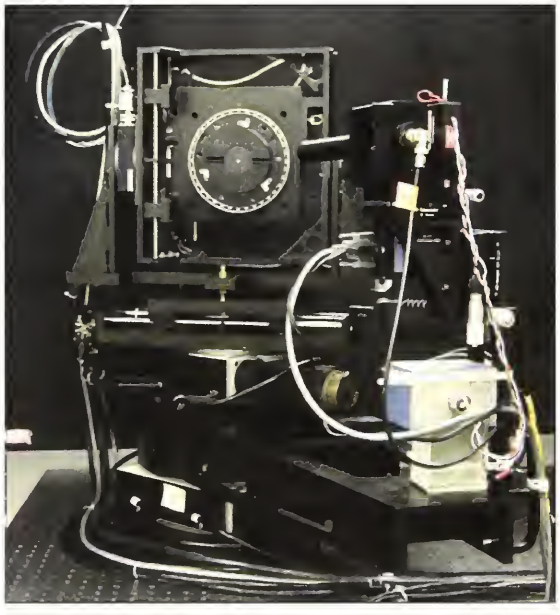

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

DELIVERABLES: Perform measurements of scatter from various films to assess the particle detection limits on those films. 3Q 2006

2. Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with diclectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES: Publish response curves for a variety of scattering geometries for particles on wafers with blanket films. 3Q 2006

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle size below 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Deliver a 100 nm particle size SRM to replace SRM1963 and a 60 nm particle size SRM. 2Q 2006

4. Resource on Particle Science – Over the past five years, the particle-related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Provide technical support to the SEMI Advanced Wafer Surface Inspection System task force. 3Q 2006

Accomplishments

- Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

- Developed a NIST Calibration Facility for sizing monodisperse spheres suspended in water in the size range of 50 nm to 400 nm with an expanded uncertainty of 1.5 % of the peak size. This facility has been used for two customers providing calibration particles to the semiconductor community.

- Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

- In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

- Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

- Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 3300 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating integrated scatter, was released in June 2004.

- Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

- Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

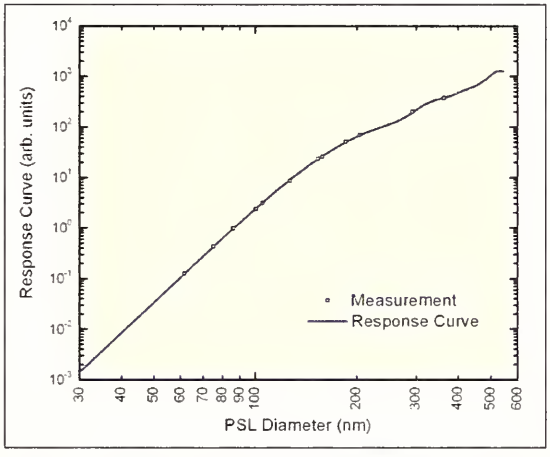

Figure 2. Sample calibration of a commercial wafer scanner using the new SEMI M53 method. The relative expanded uncertainty in particle diameter has been reduced to less than 1 %.

- Assisted in revising SEMI M53, a practice for calibrating scanning surface inspection systems, by developing a model-based calibration scheme that matches measured signals from PSL spheres to the predictions of a theoretical model. The accepted model for scattering by the spheres is specified in the standard as that provided by the MIST program. The new method has several advantages over the previous method, including: less sensitivity to changes in availability of specific size standards, improved accuracy, less variability between instruments, and an ability to extract a quantitative accuracy from the calibration. The expanded uncertainty found by applying the calibration to a commercial instrument was better than 1 % of the diameter.

Collaborations

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

Thomas A. Germer, "Measuring Interfacial Roughness by Polarized Optical Scattering," in *Light Scattering and Nanoscale Light Scattering*, Alexei A. Maradudin, Ed., (Elsevier, New York, 2006) in press.

Thomas A. Germer and George W. Mulholland, "Particle Size Metrology: Comparison Between Aerosol Electrical Mobility and Laser Surface Light Scattering Techniques," in *Characterization and Metrology for ULSI Technology 2005*, D.G. Seiler, A.C. Diebold, R. McDonald, C.R. Ayre, R.P. Khosla, S. Zollner, and E.M. Secula, eds., Proc. AIP **788**, 579–583 (2005).

Jung Hyeun Kim, Sheryl H. Ehrman, George W. Mulholland, and Thomas A. Germer, "Polarized light scattering by dielectric and metallic spheres on oxidized silicon surfaces," Appl. Opt. **43**(3), 585–591 (2004).

J. H. Kim, S. H. Ehrman, and T. A. Germer, "Influence of particle oxide coating on light scattering by submicron metal particles on silicon wafers," Appl. Phys. Lett. **84**(8) 1278-1280 (2004).

J. H. Kim, S. H. Ehrman, and T. A. Germer, "Influence of particle oxide coating on light scattering by submicron metal particles on silicon wafers," Appl. Phys. Lett. **84**(8) 1278-1280 (2004).

Thomas A. Germer and Michael J. Fasolka, "Characterizing surface roughness of thin films by polarized light scattering," in *Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies*, A. Duparré and B. Singh, Eds., Proc. SPIE **5188**, 264–275 (2003).

Jung Hyeun Kim, Thomas A. Germer, Valeri I. Babushok, George W. Mulholland, and Sheryl H. Ehrman, "Co-Solvent Assisted Spray Pyrolysis for the Generation of Metal Particles," J. Materials Research, **18**(7), 1614–1622 (2003).

Thomas A. Germer, "Scattering by slightly non-spherical particles on surfaces," in *Seventh Conference on Electromagnetic and Light Scattering by Nonspherical Particles: Theory, Measurements, and Applications*, T. Wriedt, Ed. (Universität Bremen, Bremen, 2003), pp. 93–96.

Front-End Materials Characterization

Goals

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. Major focus is placed on metrology requirements from the 2004 Update to the International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) Structural and elemental analysis at the device level, including SIMS and HRTEM, and (2) Metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project defines optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high-κ and low-κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. High Resolution Transmission Electron Microscopy (HRTEM) is being developed as a chemical tomography tool for determining 3-D elemental distributions in advanced materials.

(3) Determine the work function, band offset, and interfacial structures of high-κ combinatorial metal electrode stacks systems by implementing a combination of techniques including Scanning Kelvin Probe Microscopy (SKPM), internal photoemission (IPE), backside FTIR, and external photoemission (Soft XPS and Inverse photoemission), and theoretical modeling.

Customer Needs

The Front-End Materials Characterization project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack processes and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2005 International Technology Roadmap for Semiconductors (ITRS) near-term (through 2009) difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization, introduction of metal gate electrodes with appropriate workfunctions, and metrology issues associated with 2-D dopant profiling. Metrology needs for Thermal/thin films, Doping Technology, SOI, and strained-silicon are discussed in the Metrology section of the 2005 ITRS.*

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

The ITRS identifies structural and elemental analysis at devices dimensions (for example 3-D dopant profiling) as one of the difficult challenges beyond 2009. Offline secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for at-line 2-D dopant profile concentration measurements

Technical Contacts:
G. Gillen: SIMS
D. Simons: SIMS
J. Small: TEM, X-ray detectors
J. Suehle: Electrical Characterization
N. Nguyen: IPE, SE

with spatial resolution of 3.5 nm and precision of 4 % in 2005, increasing to spatial resolution of 2.8 nm or less and 2 % precision for the 2010 through 2018 timeframe. Complete specifications are given for the short term in Table 120a on pages 21–22, and for the long term in Table 120b on pages 23–24 of the 2005 Metrology section. The need for advances in image and spectral modeling for TEM and STEM applied to 3-D atomic imaging and spectroscopy is discussed under Emerging Research Materials and Devices in the Metrology section of the 2005 ITRS.

Technical Strategy

The 2005 ITRS expressed as difficult challenges: "starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams," and "measurement of complex material stacks and interfacial properties including physical and electrical properties, page 4, Table 116, Metrology Section." Our focus areas include development of refined metrology methods and standards for SIMS and TEM, developing improved X-ray detection capabilities for SEMs and electron microprobes, and the characterization of high-κ metal gate interfaces, including band offsets and barrier heights.

Structural and Elemental Analysis at the Device Level, Including SIMS and HRTEM

Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We have organized an international round robin study through ISO committee TC201 to investigate the parameters that must be controlled to make highly repeatable dose measurements of As with SIMS instruments. In addition to improved repeatability for dopants, the ITRS roadmap also requires increased SIMS detection limits for trace metal and organic contamination analysis of semiconductor devices. We are also working on novel methods to enhance detection limits for common metal contaminants by increasing the ionization efficiency during the SIMS sputtering process.

DELIVERABLE: Measure detection limits of selected trace metals on silicon using high transmission/high mass resolution SIMS system. 3Q 2006

Analysis of trace metal and organic contamination on silicon surfaces is a high priority of the ITRS roadmap. To utilize effectively tools such as secondary ion mass spectrometry for trace contamination on silicon surfaces, suitable trace standards must be developed. Over the past 20 years, piezoelectric drop-on-demand ink-jet printing has evolved into a precision microdispensing technology with a diverse range of applications. Examples of applications include desktop color printers, printing and synthesis of DNA arrays and printing of molten solder for use as electrical interconnects on integrated circuits. We are exploring the possibility of using ink-jet technology to print elemental and organic contamination standards on silicon. Piezoelectric printers are capable of printing single microdrops of fluid at the rate of thousands of drops per second. Each drop contains a known concentration of the material of interest. Large concentration ranges are possible simply by varying the number of drops printed. Our first attempts will explore ink-jet printing of organic test dyes on silicon with subsequent characterization by SIMS. Once standard operating procedures are developed for ink-jet printing, it should be feasible to produce standards, (both organic and trace metal) for quality control and calibration of a variety of analytical techniques including SIMS, XPS, AES, EPMA, TXRF and others.

DELIVERABLES: Produce prototype trace metal standards on silicon by ink-jet printing and evaluate by SIMS measurements. 3Q 2006

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low energy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster. This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction the depth of penetration of the primary ion. This process may potentially

allow for ultra high resolution depth profiling. In this project, we will utilize C_{60}^+ and Bi_3^+ cluster primary ion beam sources at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layers test materials.

Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth of the primary ion but by the topography induced by the sputtering process itself. We will also explore the use of cluster bombardment SIMS for reduction of sputter induced topography in metal films. This approach will be applied to study depth profiling analysis of gold diffusion in copper and the depth distribution of blanket metals films (copper metallization on silicon).

DELIVERABLES: Evaluate possible applications of a Bi cluster ion source for ultrashallow depth profiling. 3Q 2006

Measurement of the barrier height and determination of the band structure is not straightforward. Recent work by numerous researchers has shown that the measured band offset between a metal gate electrode and high-κ gate dielectric is dependent on numerous factors including composition, structure, and thickness of both the metal gate electrode and the high-κ dielectric. Because of limitations associated with any single technique, we believe that determination of band offsets and work functions requires the use of an array of techniques and the broad expertise available at NIST. We will focus our efforts on the following measurements: standard Capacitance-Voltage (C-V) and tunneling current-voltage (I-V) measurements, internal photoemission, Kelvin probe, and soft X-ray and inverse photoelectron spectroscopy.

DELIVERABLES: Improve efficiency of internal photo emission system and demonstrate performance on metal/high-κ Si structure to determine band offsets. 1Q 2006

Combinatorial "libraries" of candidate metal gate electrode films (on high-κ layers supplied by SEMATECH or member companies) are films in which the composition has been intentionally graded in the plane of the film, thus allowing one to explore many film compositions simultaneously. The combinatorial libraries will be subjected to a variety of thermal treatments to understand the stability of the interface. Using these libraries, we will be able to screen a wide variety of candidate metal gate electrodes. Many metals possess the appropriate work functions for use as NMOS ($\phi_m \sim 4$ eV: Al, Ta, Mo, Zr, Hf, V, Ti) or PMOS ($\phi_m \sim 5$ eV: Co, Pd, Ni, Re, Ir, Ru, Pt) metal gate electrodes. However, in their pure form, most suffer from other problems such as reactivity and/or adhesion issues with the high-κ gate dielectric. Binary or ternary alloys of these metals might be more suitable. Therefore we will investigate combinatorial libraries of alloys in the systems, for example, Ru-Hf, Ru-Ta, Ru-Mo, Pt-Al, Pt-Ni, Ta-Ru-Pt, W-Re-Pt, Al-Ta-Ru, and Co-Ni-Ti. Further, oxides, nitrides, oxynitrides and silicides of these metals and alloys (*e.g.*, RuO_2, ReO_2, HfN, TiN_x, TaN_x, Ta-Si-N) might also possess the proper work function and interfacial stability with the high-κ gate dielectric, and they will similarly be investigated. These alloys will be fabricated in blanket form which for physical characterization such as internal photo emission (IPE), spectroscopic ellipsometry, as well as with shadow masks to form capacitors for electrical characterization.

DELIVERABLES: Determine Optical constants for Ti-Ni-Pt ternary system using vacuum ultraviolet spectroscopic ellipsometry. 3Q 2006

Accomplishments

Implementation of C_{60}^+ Cluster Ion SIMS Capability

■ Previous efforts with cluster ion sources used for analyzing both organic and inorganic materials have been very successful. Minimization of beam-induced damage in organic materials has allowed depth profiling of polymers such as photoresists and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefitted in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multi-layers stacks. We have investigated the use of a commercially available C_{60}^+ ion source on the NIST magnetic sector SIMS instrument. We have produced stable ion beams of C_{60}^+ and C_{60}^{2+} with typical currents approaching 20 nA under conditions that allow for several hundred hours of operation. The beam can be focused into a spot size of ~1 μm allowing micrometer spatial scale mapping of patterned wafers. Optimal experimental conditions have been defined to allow for depth profiling analysis of silicon wafer samples, delta doped structures and metal multilayers. One of the critical issues for optimization of this source for analysis of silicon wafer samples is the primary ion impact

energy of the C_{60}^{+}. As shown in Fig. 1, we have found that at impact energies below ~12 keV, carbon deposition is the dominant process during bombardment precluding the acquisition of depth profiles from the wafer sample. Successful depth profiles are only achieved at impact energies of energies exceeding 12 keV. The deposition effect may be useful for lithographic applications as it allows direct ion beam writing of a conductive carbon layer on silicon.

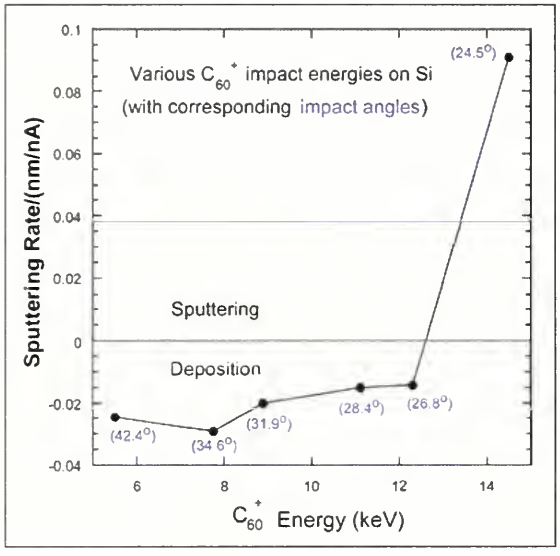

Figure 1. Sputtering or deposition rate for C_{60}^{+} on Si as a function of impact energy (angle of incidence in parentheses).

Depth Profiling of Organic Overlayers Using SIMS

■ Organic photoresists and low-κ dielectric materials are key components for front end semiconductor processing. There is also a growing interest in the use of organic semiconductor materials for organic light emitting diodes and organic thin film transistors. In anticipation of a growing need for metrology tools to characterize these types of materials, we are developing new approaches to characterize the chemical composition and in-depth distribution of organic thin films on silicon. Typically, the use of ion beam sputtering techniques, such as secondary ion mass spectrometry (SIMS), results in extensive chemical degradation of organic thin films such as photoresists or organic light emitting diodes. However, we have found that cluster primary ion bombardment SIMS can minimize this degradation allowing for intact characteristic ions to be obtained throughout the depth of the film. Furthermore, it appears that analyzing these organic materials at cryogenic temperatures provides further reduction in beam-induced damage. In this project, an SF_5^{+} polyatomic primary ion source was used to SIMS depth profile Poly(methyl methacrylate) (PMMA) photo resist at a series of temperatures from -75 °C to 125 °C where the primary glass transition for PMMA occurs at 105 °C. The depth profile characteristics (*e.g.*, interface widths, sputter rates, damage cross sections, and overall secondary ion stability) were monitored as a function of temperature. It was found that at low temperatures, the secondary ion stability increased considerably. In addition, the interfacial widths were significantly lower. Examples of this increased stability at low temperatures are illustrated in Fig. 2 for the PMMA fragment at m/z = 69. Corresponding AFM images indicated that there was also decreased sputter-induced topography formation at these lower temperatures as illustrated in Fig. 3 (page 81). Higher temperatures were typically correlated with increased sputter rates. However the improvements in interfacial widths and overall secondary ion stability were not as prevalent as was observed at low temperatures. The importance of the glass transition temperature (T_g) on the depth profile characteristics was also apparent. The results of this study demonstrate that it is possible to monitor the chemical composition of thin photoresist layers on silicon by analyzing the samples at cryogenic temperatures.

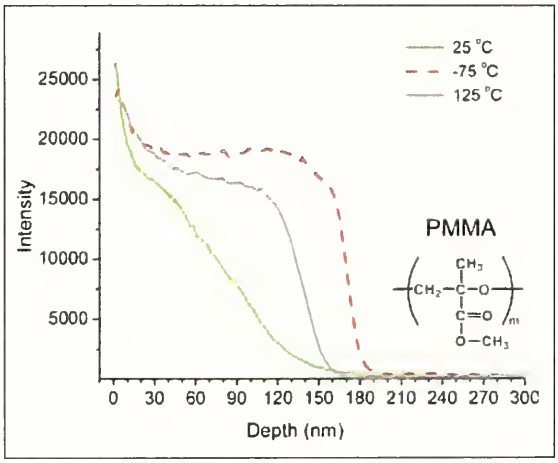

Figure 2. Positive ion intensities of characteristic fingerprint ion of PMMA m/z = 69 plotted as a function of depth for a PMMA film on Si (≈160 nm) measured at varying temperatures (at and below room temperature).

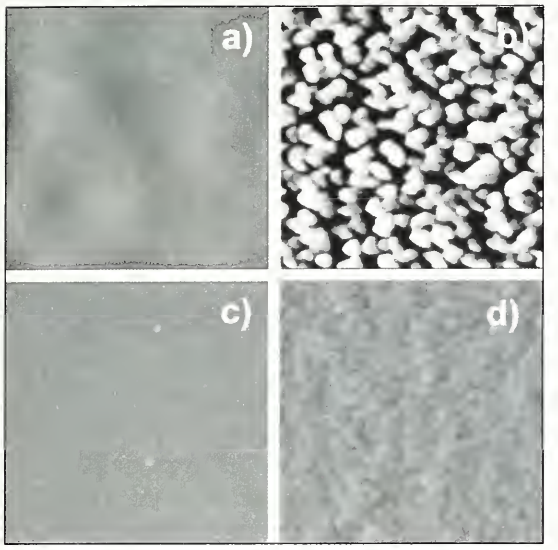

Figure 3. Atomic Force Microscopy (AFM) topography images (1 μm x 1 μm area) of SF_5^+ sputtered crater bottoms at different temperatures: (a) PMMA surface, R_{rms} = ~0.85 nm, (b) 25 °C, R_{rms} = ~11.37 nm, (c) -75 °C, R_{rms} = ~0.274 nm, and (d) 125 °C, R_{rms} = ~1.00 nm.

Si-Ge Composition Standards

■ A single-crystal boule with a nominal formula of $Si_{0.86}Ge_{0.14}$ was determined by wavelength dispersive electron probe microanalysis (WD-EPMA) to have a micro-scale expanded uncertainty no greater that 1.5 % relative mass fraction for Ge and considerably less for Si. Bulk specimens of this material were analyzed with instrumental neutron activation analysis (INAA) and inductively coupled optical emission spectroscopy (ICP-OES). The consensus mean of the two analyses using a bound on bias statistical method was 30.228 % mass fraction with a relative expanded uncertainty of 0.41 %. The quantification and heterogeneity uncertainties combined in quadrature resulted in a relative microanalysis uncertainty of 1.56 %. WD-EPMA quantification of the boule using pure Si and Ge wafer standards resulted in an average value of 30.36 % mass fraction Ge from determinations at 15, 20, and 25 kV with a maximum expanded uncertainty of 1.44 % relative. This specimen can now be used as a reliable reference standard for EMPA quantification of Si_xGe_{1-x} films on Si that are needed by industry as reference standards for their Si and Ge compositions.

Two films of Si_xGe_{1-x} on Si were prepared by the ASM America using chemical vapor deposition. The nominal compositions were $Si_{0.90}Ge_{0.10}$ and $Si_{0.75}Ge_{0.25}$ with approximate thicknesses of 4 μm and 5 μm, respectively. The purpose was to characterize the films for the extent of heterogeneity and composition and to distribute them to industry as reference composition standards. The extent of heterogeneity was determined with micrometer step traverses and with multiple point, multiple sample, and duplicate data acquisitions using WD-EPMA. The overall relative expanded heterogeneity uncertainty, including the between-specimens, between-points, and experimental components, was 1.04 % and 0.94 % for Ge in $Si_{0.90}Ge_{0.10}$ and $Si_{0.75}Ge_{0.25}$ respectively. Quantitative analysis of the two films with WD-EPMA at 20 kV, using the $Si_{0.86}Ge_{0.14}$ boule cited above as the standard, resulted in Ge concentrations of 22.72 % mass fraction ± 1.23 % for $Si_{0.90}Ge_{0.10}$ and 43.53 % mass fraction ± 1.06 % for $Si_{0.75}Ge_{0.25}$. These relative expanded uncertainties include the heterogeneity component. The overall uncertainty for the analysis, combining in quadrature the uncertainty observed for each film with that determined for the boule results in a relative expanded uncertainty of 1.98 % for the $Si_{0.90}Ge_{0.10}$ film and 1.89 % for the $Si_{0.75}Ge_{0.25}$ film. Five samples of each film will be packaged and made available to industry as NIST Research Materials before the end of FY 2006.

Round-Robin Study of Arsenic Implant Dose Measurement in Silicon by SIMS

■ An international round-robin study was undertaken under the auspices of SIMS subcommittee SC 6 of International Organization for Standardization Technical Committee TC 201 on Surface Chemical Analysis. The purpose of the study was to determine the best analytical conditions and the level of interlaboratory agreement for the determination of the implantation dose of arsenic in silicon by SIMS. Motivations for this study were: (a) the relatively poor interlaboratory agreement that was observed in a previous round-robin study before a certified reference material had become available; (b) the observation that the use of Si_3^- as a matrix species combined with $AsSi^-$ detection may result in improved measurement repeatability compared with Si_2^-; and (c) the observation that point-by-point normalization can extend the linearity of SIMS response for arsenic in silicon beyond $1x10^{16}/cm^2$.

Fifteen SIMS laboratories participated in this study, as well as two laboratories that performed Low-energy Electron-induced X-Ray Emission Spectrometry (LEXES) and one that made measurements by Instrumental Neutron

Activation Analysis (INAA). The labs were asked to determine the implanted arsenic doses in three unknown samples using as a comparator Standard Reference Material 2134, with a certified dose of 7.33×10^{14} atoms/cm^2. The use of a common reference material by all laboratories resulted in much better interlaboratory agreement than was seen in the previous round-robin that lacked a common comparator. The relative standard deviation among laboratories was less than 4 % for the medium-dose sample, and somewhat larger for the low- and high-dose samples (see Fig. 4). The high-dose sample showed a significant difference between point-by-point and average matrix normalization because the matrix signal decreased in the vicinity of the implant peak, as previously observed. The average dose from point-by-point normalization was in close agreement with that determined by INAA, indicating that the SIMS relative sensitivity factor approach is valid for arsenic concentrations in silicon as high as 4 atom percent.

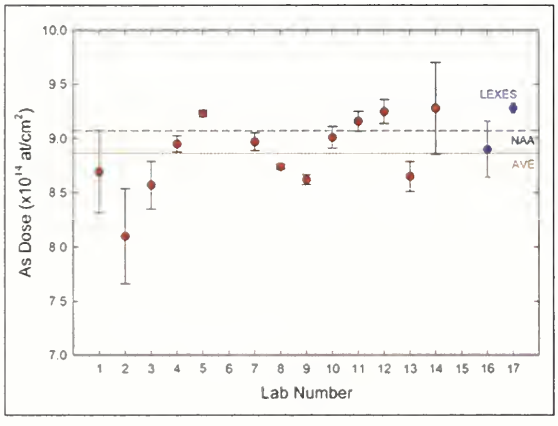

Figure 4. As round robin results for medium dose sample with point-by-point normalization to matrix signal. SIMS lab results shown in red with error bars indicating within-lab repeatability. Relative standard deviation among labs is 3.9 %. Also shown are LEXES results (blue dots), average of SIMS lab results (red line), and NAA result (black dashed line).

Enhanced Performance of Microcalorimeter X-Ray Detector

■ The NIST transition edge sensor (TES) microcalorimeter X-ray detector is a versatile instrument that combines the high resolution of wavelength-dispersive detectors with the extended range of energy-dispersive detectors. The detector is a small calorimeter operated at a low temperature (70 mK). The temperature change caused by the absorption of single X-ray photons is registered by a current through the transition edge sensor — a thin metal film that undergoes a superconducting-normal transition at the operating point. Our present detector has demonstrated a FWHM resolution of 4.4 eV at 5.9 keV. The technology of microcalorimeters is more complicated than most X-ray detectors, so that a new set of operating considerations has emerged in the process of developing it as an analytical instrument.

We report here the first operation of the NIST TES microcalorimeter X-ray detector to perform quantitative analysis of a sample with an electron probe. The detector element is mounted at the end of a probe projecting from the dewar into the electron microscope. The probe extends horizontally, which requires a sample mounting angle of 45° to optimize the yield with a vertical electron beam. The sample was analyzed using a microbeam probe with a beam current of 7 nA at an energy of 12 keV.

The detector is a microcalorimeter element 400 μm square, located approximately 30 mm from the source of the radiation. Its energy range is 400 eV to 7 keV. Count rates of 50/s to 170/s were registered while taking spectra of the sample and related standards. Spectra were processed using conventional analog pulse amplifiers and pulse-pileup circuitry modified for the relatively long period of the microcalorimeter pulses. The pulses were recorded with a 16K channel multichannel analyzer board with an approximate resolution of 0.5 eV/channel. All spectra were obtained in 1000s live time.

The sample was the K-411 glass which is part of the NIST Standard Reference Material 470, Mineral Glasses for Microanalysis, a standard intended for use with electron probe microanalysis and SIMS. It contains previously analyzed quantities of SiO_2, MgO, FeO, and CaO. Spectra were also taken of reference standards consisting of Fe, SiO_2, MgO, and chloroapatite [$Ca_5(PO_4)_3Cl$]. A spectrum of K-411 glass used in the quantitative analysis is shown in Fig. 5 (page 83).

Calculations were carried out using a Monte Carlo procedure which varied the composition of the respective elements. The maximum deviation from the concentrations certified in the NIST SRM in the first round of analysis is 2 %. The work demonstrates that the NIST TES microcalorimeter detector has considerable potential for the analysis of X-ray fluorescence lines which would overlap in current energy-dispersive detectors or would be too low in energy for most wavelength-dispersive detectors.

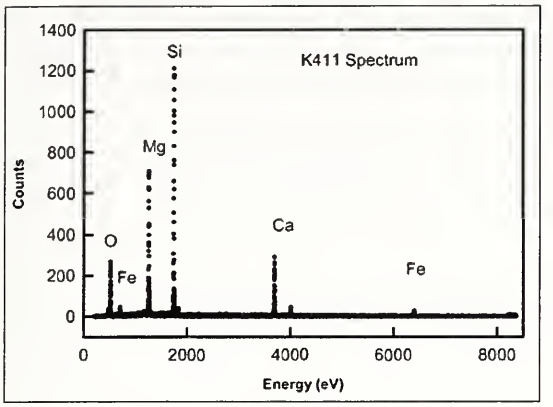

Figure 5. Spectrum of the K-411 Standard Reference Material glass taken with the NIST TES microcalorimeter X-ray detector excited by an electron beam.

Methods for Depth-sensitive Imaging by Scanning Transmission Electron Microscopy

■ As the use of data acquisition hardware capable of acquiring spectrum images becomes widespread, many analysts are employing pixel classification techniques to process their microanalysis datasets. Before the advent of spectrum imaging, analysts classified structural features in their samples using elemental X-ray maps. Today, many commercial microanalysis packages come equipped with some form of classification procedure for assigning pixels or larger spatial features to one of a small number of categories or classes. These class labels are presented to the analyst to provide insight into the chemical heterogeneity of the sample, or sometimes even its spatial distribution of "phases."

This proliferation of classification techniques within the microanalysis community has led to the need for accurate measures of performance of the various classification algorithms. Different pixel classification methods vary in their accuracy, precision, and specificity; they exhibit different strengths and weaknesses depending on the situation and what information is to be extracted from the data. The methods also exhibit different levels of sensitivity to problems in the data such as the presence of noise or badly overlapped spectral peaks. Thus, the goal of post-classification performance metrics is to illuminate how these methods meet the required analytical challenges and how gracefully their performance degrades when applied to poor or unusual data.

The best measures of performance for classifiers of all types are based on comparison of their predicted class assignments with known class membership. With real samples this is nearly impossible since the spectrum image is often the only source of phase information available at the relevant length scales. The calculation of synthetic spectrum images from computer models (Fig. 6a-e) obviates this problem, since both the composition and microstructural geometry are precisely known for the phantom samples. This allows the creation of a "ground truth" image revealing the true class membership of each pixel. Using this ground truth image as a key, the performance of any given classifier can be assessed, including measurement of error rates (both errors of commission and omission). When the classifier returns the same number of classes as the ground truth (Fig. 6f), all errors can be tabulated in a confusion matrix; when the number of classes is variable (Fig. 6g) error assessment is not as straightforward. Classifiers with thresholds as free parameters (such as Bayes classifiers) benefit from

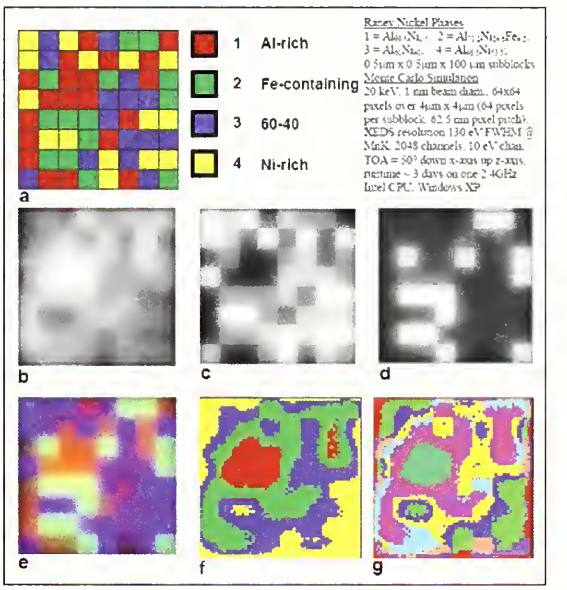

Figure 6. (a) ground truth image showing arrangement of the four Raney Nickel phases simulated by 3-D Monte Carlo; a 64 x 64 pixel spectrum image (SI) was generated with an XEDS spectrum at each pixel (b) Al K X-ray map derived from the SI (c) Ni K X-ray map (d) Fe K X-ray map (e) RGB overlay of the three elemental maps with red=Al, green=Fe, and blue=Ni (f) unsupervised pixel classification result using iterative K means and four pixel categories to classify the first 20 principal components of the SI; the poor quality of the classification is deliberate to illustrate the utility of post-classification performance metrics (g) unsupervised pixel classification result using the ISODATA iterative algorithm to classify the first 20 principal components; the number of classes is a free parameter in this algorithm, complicating measurement of classification accuracy.

analysis of their receiver-operator characteristic (ROC) curves, which reveals the relationship of false negative vs. false positive classification error rates as a function of the cut-off threshold.

Characterization of the High-κ Metal Gate Barrier Height Using Internal Photo Emission (IPE)

■ Metal gates have been intensively searched in the past few years to replace the traditional polysilicon for the next generations of MOSFET devices. One of the most important parameters used to select an appropriate metal is the barrier height (Φ_0) at the metal gate and the gate dielectric. Two important ternary metals: TaSiN and TaCN on either SiO_2 and HfO_2 were studied. Using internal photoemission, we were able to determine the barrier heights between these metals and dielectrics. As a result, $\Phi_0 = 3.36$ eV and 3.55 eV for TaSiN/SiO_2 and TaCN/SiO_2 interfaces, respectively. Figure 7 shows a plot of barrier height vs the square root of electric field for both metal on the HfO_2 gate dielectric. It is observed that $\Phi_0 = 2.24$ eV and 2.47eV for TaSiN/HfO_2 and TaCN/ HfO_2 interfaces, respectively. It is observed that the difference in the barrier heights of both metals is about 0.2 eV on either of the dielectrics. This indicates that no Fermi pinning is evident at the HfO_2 interfaces.

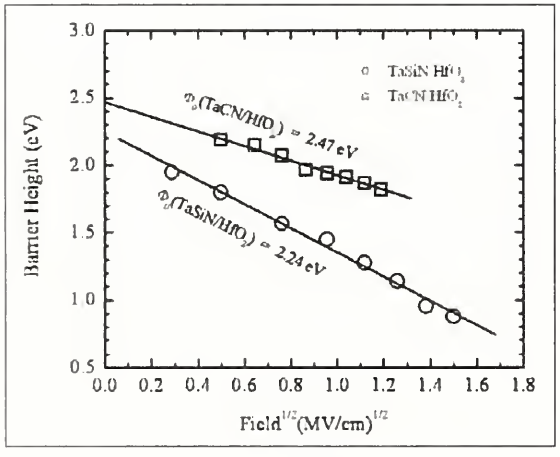

Figure 7. Plot of barrier height vs the square root of electric field obtained from internal photo emission experiments. The barrier heights differ by approximately 0.2 eV.

Film Thickness Dependence of Sub-bandgap Defect States Observed in Polycrystalline Hafnium Oxide

■ In collaboration with IBM we compare hafnium-based high-κ dielectric films grown by MOCVD and ALD. MOCVD-grown HfO_2 films are mostly monoclinic, while HfSiO films are amorphous. Thin ALD-grown HfO_2 films are amorphous, while thick films are monoclinic, with traces of orthorhombic or tetragonal phase present. Fig. 8 shows that sub-bandgap absorption is observed in polycrystalline, but not in amorphous, films. We note that sub-bandgap states may be the underlying cause for gate leakage via Frenkel-Poole hopping. The addition of Si to HfO_2 reduces the tendency for crystallization, mitigating such issues. However, such sub-bandgap states likely will not be a limiting factor in high-κ based CMOS technologies, since they line up close to the band edge and are therefore not accessible at the low gate voltages employed.

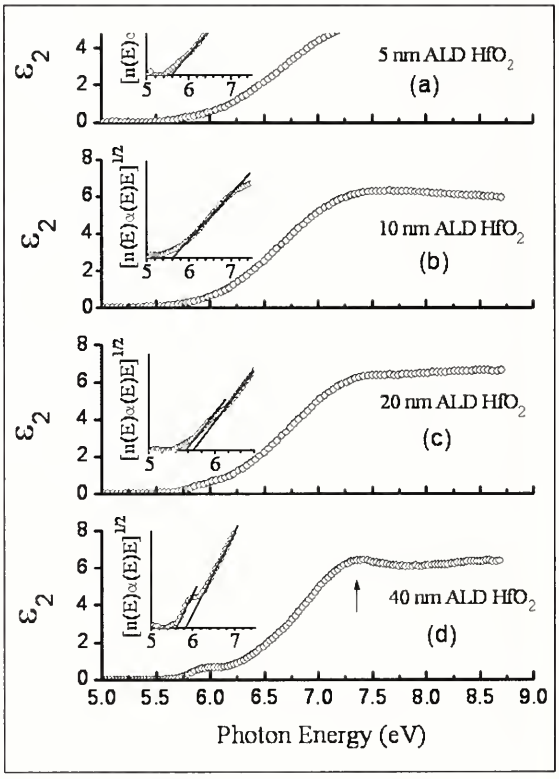

Figure 8. The imaginary part of the dielectric function, determined from VUV-SE data, for 5, 10, 20, 40 nm thick ALD HfO_2 films. All MOCVD HfO_2 spectra (not shown) are similar to that of the polycrystalline 40 nm ALD HfO_2 sample. All MOCVD HfSiO spectra (not shown) are similar to that of the amorphous 5 nm ALD HfO_2 sample.

Collaborations

International SEMATECH, Joe Bennett – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers

Ionoptika – Development of a C_{60}^+ primary ion source for advanced semiconductor technology

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces

Peabody Scientific – Ion source development for Semiconductor SIMS

SEMATECH, Characterization of metal gate/high-κ systems.

University of Maryland, College Park, Ultra-thin gate oxide reliability.

MSEL, Characterization of metal gate/high-κ systems.

IBM, Electrical characterization of high-κ systems.

Intel, Electrical characterization of high-κ systems.

Texas Instruments, Electrical characterization of high-κ systems.

Rutgers University, Characterization of metal gate/high-κ systems.

Micron, Characterization of metal gate/high-κ systems.

Yale University, Electrical characterization of high-κ systems.

Recent Publications

D. S. Simons et al., *"Round Robin Study of Arsenic Implant Dose Measurement by SIMS,"* Appl. Surf. Sci. (2006), in press.

G. Gillen et al., *"Depth Profiling using C_{60}^+ SIMS- Deposition and Topography Development During Bombardment of Silicon,"* Appl. Surf. Sci. (2006), in press.

G. Gillen, C. Mahoney, M. Wagner and A. Fahey, *"3D Molecular Imaging SIMS,"* Appl. Surf. Sci. (2006), in press.

A. Fahey, C. Mahoney and J. Hudgens, *"Applications of the Hadamard Transform to Time of Flight SIMS,"* Appl. Surf. Sci. (2006), in press.

A. Fahey, G. Gillen, P. Chi and C. Mahoney, *"Performance of a C_{60} Ion Source on a Dynamic SIMS Instrument,"* Appl. Surf. Sci. (2006), in press.

C. M. Mahoney, A. J. Fahey and G. Gillen, *"Temperature-Controlled Depth Profiling in Polymeric Materials using Cluster Secondary Ion Mass Spectrometry (SIMS),"* Appl. Surf. Sci. (2006), in press.

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Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Atomic Layer Deposition – Process Models and Metrology

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Goals

Develop validated, predictive process models and *in-situ* metrologies for atomic layer deposition processes.

Customer Needs

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high-κ gate dielectric layers, diffusion barrier layers, copper seed layers, and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the *2005 International Technology Roadmap for Semiconductors (ITRS)* as *"one of the few enabling methodologies that can reduce development cycle times and costs."* [*2005 ITRS, Modeling and Simulation, page 1*] A TCAD topical area identified in the 2005 ITRS is *"Equipment/feature scale modeling—hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings."* [*2005 ITRS, Modeling and Simulation, page 1*] A difficult challenge related to this topical area is *"Integrated modeling of equipment, materials, feature scale processes and influence on devices"* [*2005 ITRS, Modeling and Simulation, Table 122, page 2*] with associated issues including *"Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms, and simplified but physical models for complex chemistry"* and ALD deposition modeling. [*2005 ITRS, Modeling and Simulation, Table 122, page 2*] In addition, the 2005 ITRS notes that *"a key difficult challenge across all modeling areas is that of experimental validation."* [*2005 ITRS, Modeling and Simulation, page 1*] Further, with respect to experimental validation, *"One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films."* [*2005 ITRS, Modeling and Simulation, page 17*]

This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and associated *in-situ* metrologies for ALD processes.

Technical Strategy

ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the gas flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of custom-built, research-grade ALD reactors with optimized optical accessibility and benchmarking the numerical results with experimental data. These data are obtained using various measurement techniques, including vibrational spectroscopies and mass spectrometry. HfO_2 ALD using tetrakis(ethylmethylamino) hafnium (TEMAH) and water has been selected as the chemical system for primary investigation.

This project involves two general directions of investigation: development of *in-situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that the important reaction species will be identified as the understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

1. The first step in providing validated ALD process models is evaluating the suitability of

diagnostics that are sensitive to ALD chemistry. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their potential for *in-situ* monitoring. While sensors that are sensitive to gas phase species (*e.g.*, mass spectrometry and Fourier-Transform infrared (FTIR) spectroscopy) are easier to integrate into commercial reactors (*e.g.*, in the gas exhaust line), these techniques are only sensitive to volatile species. Hence, it is sometimes difficult to relate the species detected with such techniques to mechanisms of interest on the growth surface. Hence, both gas-phase-sensitive and surface-sensitive techniques are being evaluated to probe ALD chemistry. The suitability of Raman spectroscopy and FTIR spectroscopy for probing ALD surface processes under actual deposition conditions is being investigated. In addition, the suitability of mass spectrometry and FTIR spectroscopy for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. Research-grade ALD reactors with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques have been designed and constructed.

DELIVERABLES:

- Complete evaluation of fiber-optic coupled, polarized, *in-situ* Raman spectroscopic measurements for probing ALD surface processes. 3Q 2006
- Complete evaluation of time-resolved, *in-situ* FTIR measurements for probing ALD gas phase processes. 3Q 2006
- Interface mass spectrometer with ALD chamber. 4Q 2006

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD and chemical vapor deposition (CVD) is an important aspect of this project and is an ongoing process. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity compiles and evaluates currently available thermochemical and chemical kinetic data for organometallic compounds and related precursors. The second activity supplements available data by using *ab initio* and semi-empirical quantum calculations coupled with transition state calculations to develop detailed chemical kinetic models from computed molecular structures, thermodynamic properties and spectroscopic properties of relevant compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop detailed chemical kinetic models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES:

- Compilation of bibliography pertaining to ALD and CVD systems. Make this information available through the Standard Reference Data website. Ongoing
- Perform high level ab initio quantum calculations for HfO_2 precursors and derivatives to benchmark heats of formations and bond dissociation energies. 3Q 2006
- Develop simple model for HfO_2 ALD from TEMAH and water. 4Q 2006

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of *ex-situ* film characterization measurements to reactor conditions as determined by *in-situ* measurements and numerical modeling of the temperature and flow fields in the reactor. *In-situ* measurement techniques include those techniques being developed for model validation. *Ex-situ* measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy (XPS), X-ray diffractometry, atomic force microscopy, and ultraviolet Raman spectroscopy. The data provided by these measurements, spatially resolved when possible, would include such film characteristics as thickness, stoichiometry, HfO_2 phases present, and degree and type of impurity incorporation.

DELIVERABLES: Investigate the relationship between ALD process parameters, reactor gas flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics. Ongoing

Accomplishments

■ ALD Reactor Modeling — Three dimensional CFD models for gas flow and temperature fields have been developed for various reactor geometries, including optically-accessible reactor designs, and used to model flow and temperature under various process conditions, as shown in Fig. 1.

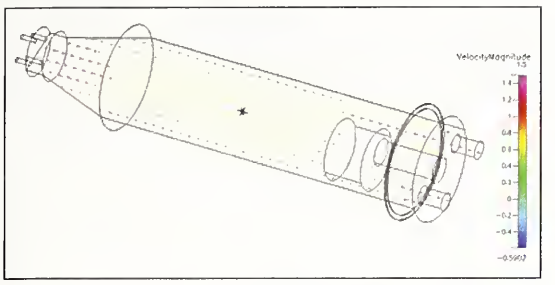

Figure 1. A two dimensional gas velocity profile slice obtained from a full three dimensional reactor model.

In addition, time-resolved precursor distributions have been modeled, as shown in Fig. 2.

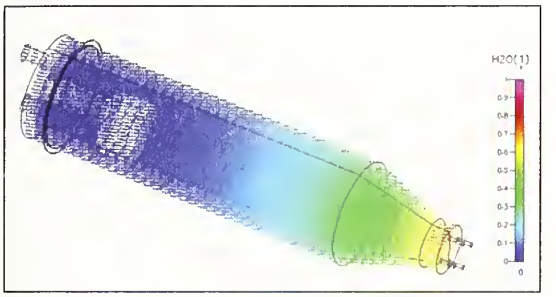

Figure 2. A three dimensional mass fraction profile showing water mass fraction distribution 0.1 sec after water injection into the reactor.

The results from these models have been used to help optimize reactor designs, especially optical window design, and deposition conditions. Chemical reaction mechanism models for HfO_2 ALD are being developed for use with these three dimensional flow and temperature models to simulate the entire ALD process.

■ HfO_2 ALD — Research-grade, optically-accessible ALD reactors have been designed and constructed with full optical access for surface and gas-phase Raman and FTIR spectroscopic measurements. An associated pulsed gas delivery system has been designed and constructed. Using this deposition equipment, ALD HfO_2 films have been deposited under a variety of process parameters using TEMAH and water or tetrakis(dimethylamino) hafnium (TDMAH) and water. Films have been characterized with a number of techniques, including VUV-SE and XPS, as shown in Fig. 3 and Fig. 4, respectively.

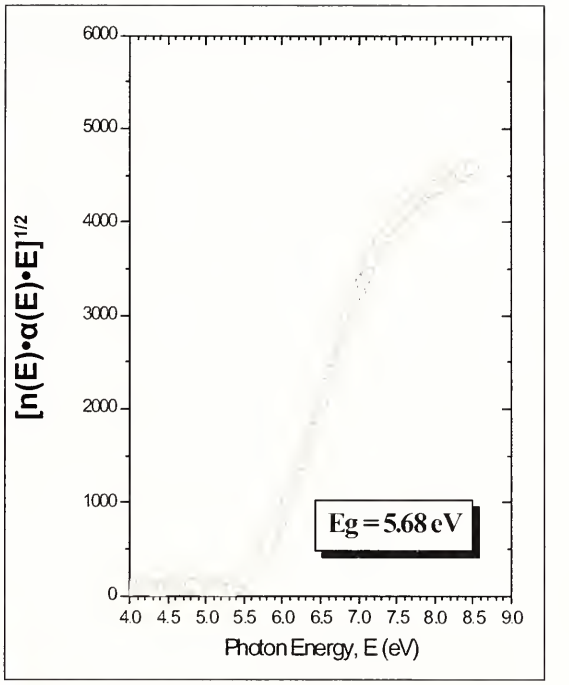

Figure 3. Imaginary part of the complex dielectric function as a function of photon energy for HfO_2 ALD film as determined using VUV-SE. The inset illustrates determination of band gap energy by extrapolation of the expression $[n(E)•\alpha(E)•E]^{1/2}$ to zero (data courtesy of N.V. Nguyen).

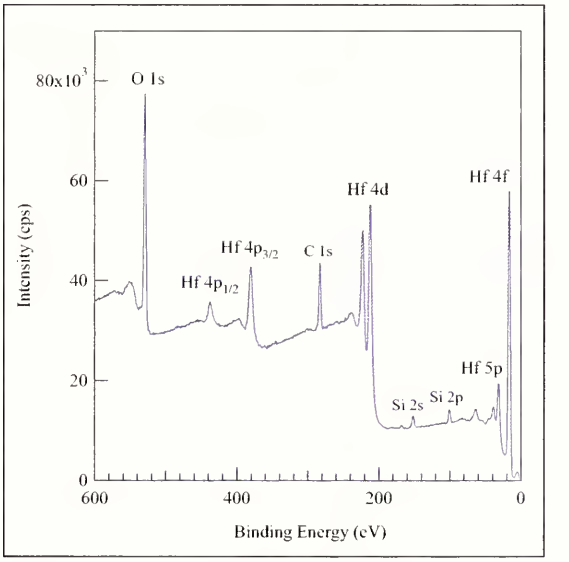

Figure 4. X-ray photoelectron spectrum of HfO_2 ALD film (data courtesy of K.L. Steffens).

■ *In-Situ* Optical Measurements — *In-situ* gas phase FTIR measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to deposition reactants, TEMAH, and products, N-methylethylamine, as illustrated in Fig. 5 (page 92).

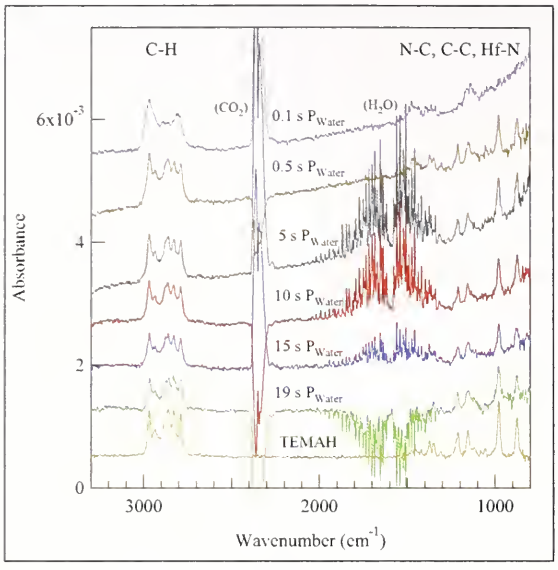

Figure 5. Gas phase FTIR spectra as a function of purge time following a water pulse.

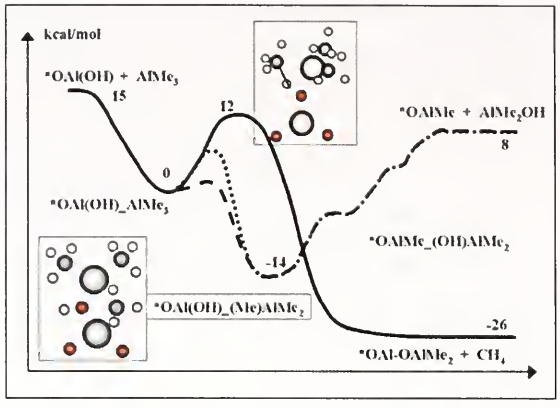

Figure 6. Calculated potential energy surface for reaction of trimethyl aluminum with a hydroxylated aluminum oxide cluster.

In addition, *in-situ* FTIR measurements during TEMAH injection pulses were shown to be sensitive to TEMAH decomposition in the delivery system. *In-situ* surface Raman spectroscopic measurements are on-going. Excitation wavelengths are being varied and polarization analysis employed to determine maximum sensitivity to ALD species.

- Chemical Properties Calculations — Molecular structures and energies for precursors, adsorbates, intermediates, and transition states have been calculated using ab initio and density functional theory quantum calculations for ALD of Al_2O_3 from TMA and water and HfO_2 from TEMAH or TDMAH and water. Although the primary focus of this work is on HfO_2 ALD, Al_2O_3 ALD is also being investigated as a model system for two main reasons. First, there has been significant work on Al_2O_3 ALD, and consequently, there are adequate experimental data for use in chemical mechanism validation. Second, aluminum is more amenable to quantum calculations than hafnium, a transition metal. It is expected that lessons learned in developing an ALD model for Al_2O_3 ALD will be useful in development of a HfO_2 ALD model.

For Al_2O_3 ALD, prototypical small cluster ($Al_xO_yH_z$) species have been utilized to represent the surface layer. Rate expressions based on calculated structures and energies have been derived using transition state theory, as illustrated in Fig. 6.

A detailed chemical kinetic model for ALD of Al_2O_3 from TMA and water has been constructed based on these rate expressions. This model is being refined based on further reactor model simulations, comparison with experimental observables, and supplemented with additional quantum calculations, where necessary. High level ab initio calculations, up to CCSD(T)/aug-cc-pVnZ (n=2-4) have been done for small species to benchmark heats of formation and bond dissociation energies for AlH_nX species (n = 0-2, X = H, F, Cl, OH, NH_2, CH_3). Additional calculations will be done to provide higher level corrections (*e.g.*, core-valence, relativistic, etc).

Adequate reference spectra could not be located for TEMAH or N-methyl-ethanamine (MEA), a gas phase product of the TEMAH and water ALD reaction. Hence, infrared and Raman vibrational frequencies were calculated with Density Functional Theory using the B3LYP/LANL2DZ method. The calculated frequencies were compared to experimental infrared spectra obtained in the ALD reactor and tentatively identified as TEMAH and MEA, as shown in Fig. 7.

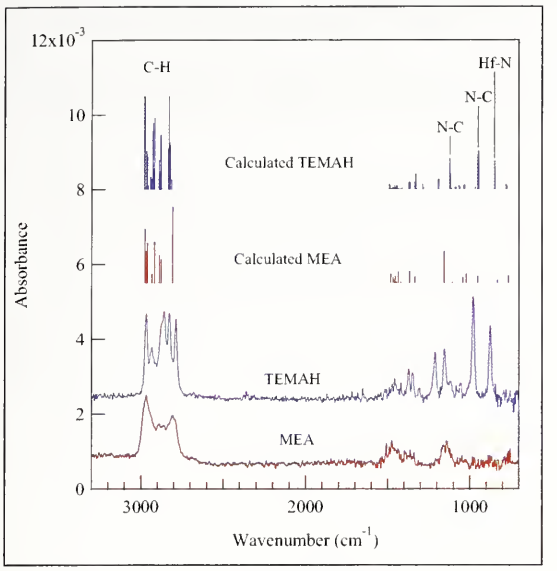

Figure 7. Comparison between calculated and experimental spectra of TEMAH and MEA.

In the infrared spectra, vibrational modes in the CH wavenumber range were scaled by 0.95 and the modes in the lower wavenumber range were scaled by 0.961.

- Database Website — A Website http://srdata.nist.gov/ckmechx/ (external) and http://h105097.nist.gov/ckmechx (internal) has been made available through the NIST Standard Reference Data website. This site currently contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, Al_2O_3, and other related ALD systems (*e.g.*, Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions.

Recent Publications

J. E. Maslar, W. S. Hurst, D. R. Burgess, Jr., W. A. Kimes, and N. V. Nguyen, "*In-Situ* Characterization Of Gas-Phase Species Present During Hafnium Oxide Atomic Layer Deposition," Electrochemical Society Transactions, 2006, in press.

D. R. Burgess, Jr., J. E. Maslar, W. S. Hurst, E. F. Moore, W. A. Kimes, and N. V. Nguyen, "Atomic Layer Deposition Process Models and Metrologies," *Characterization and Metrology for ULSI Technology: 2005 International Conference*, edited by D. G. Seiler et al., AIP Conference Proceedings 788, Melville, NY: American Institute of Physics, pp. 141-146, 2005.

Superconformal Deposition: Copper and Advanced Interconnect Materials

Technical Contacts:
D. Josell
T. P. Moffat

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations, examining the generality of the superconformal filling mechanism and exploring processes utilizing novel barriers and/or seed geometries.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever smaller dimensions has led to the rise of new challenges, including fabrication of ever thinner copper seeds, which are required for the copper superfill process, and increased resistivities of the metallizations due to size effects. To overcome these hurdles the National Institute of Standards and Technology (NIST) is enhancing existing copper technology through improved understanding and metrologies for the superfill process, examining new interconnect materials, and pursuing new fabrication techniques such as seedless processing and atomic layer deposition.

Interconnect metallization issues are discussed in the Interconnect section of the 2005 update of the International Technology Roadmap for Semiconductors.

Technical Strategy

To meet future industrial needs, we have, over the life of this project, developed metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. The derived Curvature Enhanced Accelerator Coverage (CEAC) mechanism has served as a platform for this understanding. We have also developed electrolytes and processes for superconformal deposition of advanced interconnect materials such as silver (the only metal with a higher conductivity than copper) and gold (a metallization for wide-bandgap semiconductors) as well as alternative processing schemes such as chemical vapor deposition. Research results for this year are summarized below.

In addition to the electrodeposited copper conductor itself, current metallization technology employs a barrier metal and a PVD copper seed. As feature sizes continue to shrink, the resistive barrier materials negatively impacts electrical performance and deposition of, and on, the PVD seed becomes problematic. These difficulties are driving a search for alternative barrier/wetting layer materials and processes. Ruthenium is one focus because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers, it is immiscible with copper, and copper can be electroplated directly on ruthenium, eliminating the need for the PVD copper seed layer and the corrosion problems that come with it.

Our work has explained the sensitivity of filling of ruthenium coated trenches to the manner in which the ruthenium surface is treated prior to plating, demonstrating correspondence between the surface state and the wetting and filling of ruthenium coated trenches (Fig. 1).

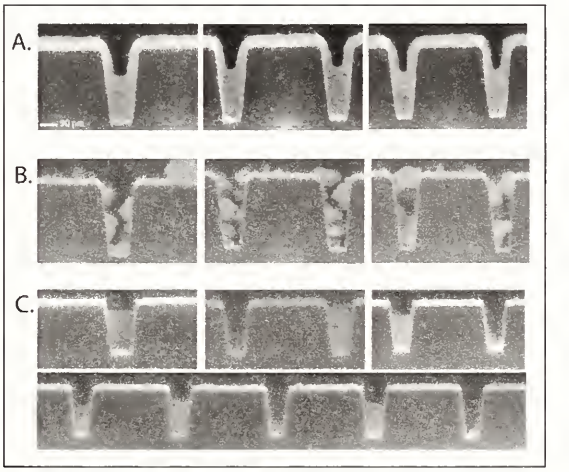

Figure 1. Nucleation and growth of copper on ruthenium is sensitive to the initial surface state. Three limiting behaviors are shown: (A) Exemplifies the desired result of early coalescence of the electrodeposited copper followed by bottom-up superfilling that is characteristic of growth on a conventional copper seed-layer, (B) poor trench filling characteristic of Volmer-Weber growth mode on poorly wetting, oxidized ruthenium and (C) selective growth within the feature that is observed sporadically in a few specimens.

We have used voltammetry to demonstrate that the absence of a two-dimensional wetting layer of "underpotential deposited copper" on oxidized ruthenium surfaces is associated with copper deposition by the undesirable Volmer-Weber growth mode and poor filling visible in Fig. 1B. Voltammetry and ellipsometry have been used to fully explore adsorption on ruthenium of additives required for copper superfill in conventional structures. The understanding of the competitive dynamic of multicomponent adsorption and consumption and its connection with microstructural and morphological evolution provided by this work will facilitate establishment of a robust manufacturing process. Metrology for assessing surface quality that is compatible with the electrochemical process used for interconnect fabrication (Fig. 2) and techniques for repairing oxidized surfaces are also detailed.

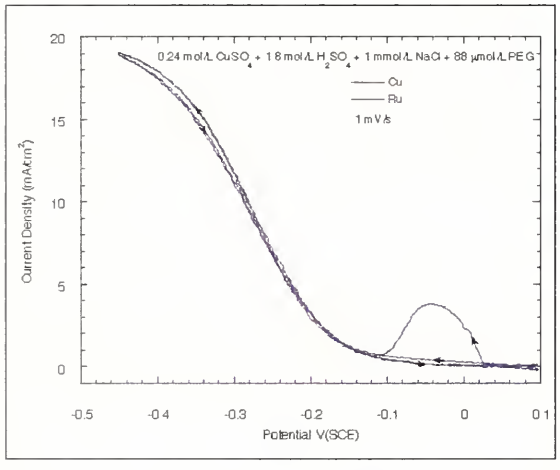

Figure 2. Deposition on oxidized and oxide-free ruthenium surfaces yields substantially different deposition signatures in superfilling electrolyte. Competition between transport-limited adsorption of suppressing additive and rapidly increasing surface area of the discrete copper nuclei that form on the oxide-coated surface yields a bump in the current-voltage trace that is a unique signal of the poor wetting visible in Fig. 1B. A smooth trace essentially identical to that for deposition on a copper surface is obtained for deposition on activated ruthenium surfaces.

DELIVERABLES: Publications detailing (1) voltammetry for assessing wettability of ruthenium surfaces, including the role of additives during superfilling of patterned features, and (2) ellipsometry to independently quantify the adsorbate coverages for comparison with the results of the electroanalytical measurements.
1Q 2006 and 2Q 2006

As feature widths and seed-layer dimensions decrease, implementation of atomic layer deposition (ALD) is being considered for seed and/or barrier deposition. We focused our efforts on seedless superfilling with ALD ruthenium and iridium coated features through a collaboration with the University of Helsinki (Fig. 3). We used PVD osmium coated features to further examine the impact of oxidation and processing on wettability and superfilling in seedless processing.

Figure 3. Trenches superfilled with copper electrodeposited directly on an ALD iridium layer. The insert shows a higher magnification view of the iridium layer; a thin alumina adhesion layer is visible underneath it.

DELIVERABLES: Publications detailing seedless superfilling of copper on PVD and ALD layers.
1Q 2006

We also extended our CEAC mechanism to probe the coupling of area change and the traditional diffusion-adsorption-consumption model of leveling. A code that includes competition of suppressor, catalyst, and leveler for surface sites in prediction of metal deposition and shape change (operating on the freeware Python platform) was used with experimentally derived kinetics to predict the impact of the leveling additive PEI on overfill bump formation (Fig. 4, page 97). The predictions capture the observed reduction of overfill bump height upon addition of leveler. Enhanced coverage of deposition-suppressing leveler through area-reduction within the CEAC mechanism also explains the observed inversion, upon addition of leveler, of relative bump heights over regions with high and low densities of superfilled features (*i.e.*, why a higher bump is observed over isolated features in the presence of leveler rather than over

grouped features as in its absence). These results have substantially improved understanding of the competitive dynamic that underlie empirical strategies of adding leveling additives to superfilling electrolytes in order to reduce overfill bump formation. The work will benefit post-plating planarization.

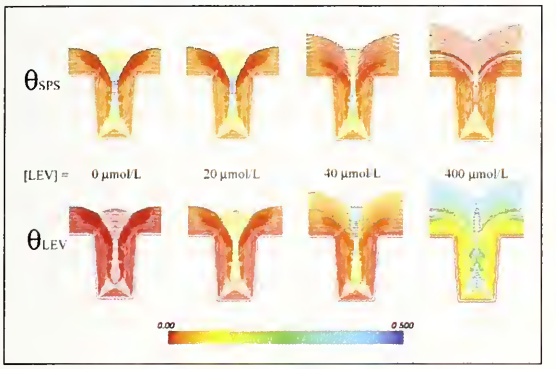

Figure 4. Simulations of feature filling as a function of the concentration of leveling additive in the electrolyte. The predictions are obtained using kinetics of the leveler PEI in a CEAC model that includes competitive adsorption of suppressor, accelerator, and leveler additives. Dilute leveler reduces the overfill bump height; higher concentrations destroy the superfill dynamic.

DELIVERABLES: Publication detailing extended CEAC formalism for modeling of electrolytes containing leveling additives as well as metrology for assessing kinetics of adsorbate interactions. 1Q 2006 and 4Q 2006

We also built upon last year's demonstration of gold superfill for fabrication of gold interconnects for III-V semiconductors such as GaAs and GaN. This effort included quantitative assessment and description of the kinetics of gold superfill with a lead accelerator. Experimental trench filling results compared favorably with the CEAC derived predictions.

DELIVERABLES: Publication detailing assessment of gold superfill kinetics with comparison of observations and CEAC predictions. 1Q 2006

Accomplishments

- We demonstrated the use of ruthenium, iridium and osmium, PVD and ALD, as interconnect surfaces compatible with superconformal electrodeposition of copper without the need for a copper seed layer. We also established metrology for assessing the state of the surface with regard to wettability and effective seedless superfill.
- We extended the existing CEAC model of superfill to include leveling additives in the electrolyte, describing metrology for assessing the kinetics of the competitive adsorption process. We also explored the impact of leveling additives on overfill bump formation during trench filling.
- We quantified bottom-up superfilling of trenches with gold that might find use in the formation of contacts and metallizations for compound semiconductors.

Collaborations

D. Wheeler, J.E. Bonevich, L.J. Richter, M.L. Walker, P.J. Chen, W.F. Egelhoff: NIST.

Christian Witt: Cookson-Enthone.

T. Aaltonen, M. Leskelä and M. Ritala: University of Helsinki.

Recent Publications

M. Walker, L. J. Richter, D. Josell and T. P. Moffat, *"An ellipsometric Study of the Cl-induced Adsorption of PEG on Ru and Cu UPD/Ru,"* Journal of the Electrochemical Society 153(4), C235-C241 (2006).

D. Josell, J. E. Bonevich, T. P. Moffat, T. Aaltonen, M. Ritala and M. Leskelä, *"Iridium Barriers for Direct Copper Electrodeposition in Damascene Processing,"* Electrochemical and Solid-State Letters 9(2), C48 (2006).

D. Josell, C. Witt and T. P. Moffat, *"Osmium Barriers for Direct Copper Electrodeposition in Damascene Processing,"* Electrochemical and Solid-State Letters 9(2), C41-C43 (2006).

T. P. Moffat, D. Wheeler, S. K. Kim and D. Josell, *"Curvature Enhanced Adsorbate Coverage Model for Electrodeposition,"* Journal of the Electrochemical Society 153(2), C127-C132 (2006).

T. P. Moffat, M. Walker, P. J. Chen, J. E. Bonevich, W.F. Egelhoff, L. Richter, C. Witt, T. Aaltonen, M. Ritala, M. Leskelä and D. Josell, *"Electrodeposition of Cu on Ru Barrier Layers for Damascene Processing,"* Journal of the Electrochemical Society, 153(1), C37-C50 (2006).

D. Josell, D. Wheeler and T. P. Moffat, *"Gold Superfill in Sub-Micrometer Trenches: Experiment and Prediction,"* Journal of the Electrochemical Society 153(1), C11-C18 (2006).

T. P. Moffat and D. Josell, *"Seedless Superfilling: Opportunities and Challenge,"* invited article in Semiconductor FabTech 27th Edition, 133-136 (2005).

Interconnect Materials and Reliability Metrology

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Basic Materials Properties
- Test Structures for Interconnect Metrology and Modeling

Basic Materials Properties

Technical Contacts:
D. Read
B. Keller

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin interconnect conducting and insulating films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses and strains, fatigue, fracture resistance, and thermomechanical response, in specimens fabricated and sized like materials used in actual commercial devices; and (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 11 thin-film layers now, and will reach 14 layers in the long term *(International Technology Roadmap for Semiconductors, 2005, Interconnect, Tables 80a-b)*. These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2005), Interconnect, p. 45, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated.* The 2003 NEMI *(National Electronics Manufacturing Initiative) Research Priorities* document reports a similar need. In a section beginning on page 24, entitled *Modeling, Simulation and Design Tools, Emerging Areas for Electronics Packaging*, Table 3, *Projected Development and Research Needs for Simulations in Emerging Areas*, includes nanoscale modeling and simulation as an area, experimental tools capable of measuring electrical, thermal, and mechanical phenomena/material properties at smaller scale as a need, and *"Issue: how is the property and behavior different from bulk behavior/macro-scale?"* as a comment. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition, electrodeposition, or spin-on deposition, their microstructures, and hence their mechanical properties, are different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results. Industry needs test methods that are efficient and integrable in the fab environment. We see nanoindentation and high-amplitude a.c. measurements as candidates to become routine, or perhaps even on-line, methods. Compared to these, the microtensile test is more laborious, but it provides unambiguous results. We will continue to promote and offer the microtensile test as a reference method, while developing methods to extract needed material property information from the more integrable methods such as nanoindentation and high-amplitude a.c. testing.

We are also working on TEM- and SEM-based techniques for measurement of local strains, to provide detailed information about the nature of deformation and stress-strain response in the dimensionally-constrained materials that make up microelectronic systems. The techniques are based on electron diffraction measurements of lattice parameters and have spatial resolutions that are compatible with state of the art device dimensions.

Electron backscatter diffraction (EBSD) offers a means by which such strains may potentially be mapped with near-20 nm resolution, since the technique is integrated with the scanning action of a SEM. Convergent-beam electron diffraction (CBED) is a TEM technique that can potentially measure strains with better than 5 nm spatial resolution, but requires specimen thinning, and is therefore subject to artifacts. We have efforts underway to advance both approaches.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology. We held a workshop entitled Reliability Issues in Nanomaterials, 17–19 August 2004, to gauge customer interest in the available tools for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests. The referenced report gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering. We are in the early stages of planning the second such workshop, to gauge progress in development of reliability metrology applicable to microelectronics and nanomaterials, and to update metrology needs that could be addressed by NIST.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand. We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry.

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue and measurements. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the SEM. This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

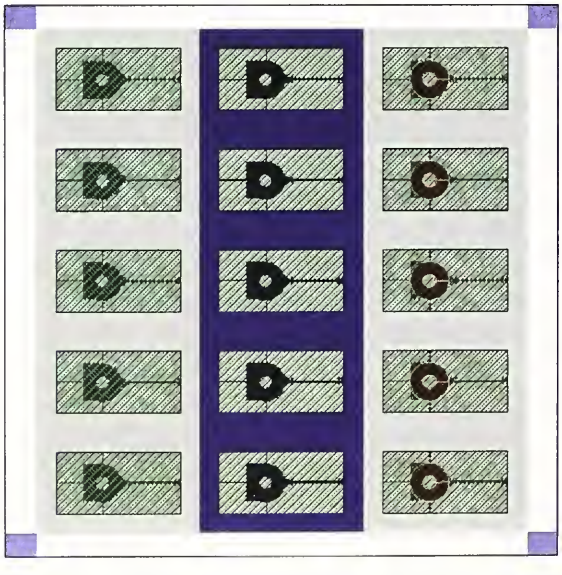

Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

DELIVERABLES: We are organizing a one-day short course consisting of 6 lectures by NIST staff on Interconnect-Relevant Characterization & Metrology, in conjunction with the 2006 Advanced Metallization Conference. 4Q 2006

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including EBSD, SEM, and TEM has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small.

We have recently presented the first set of experimental data comparing the results of high amplitude a.c. testing and tensile testing on the same material.

DELIVERABLES: Technical publication comparing results of high amplitude a.c. and microtensile testing on e-beam-deposited aluminum, in review. 2Q 2006

The initial ultimate strength value deduced from the a.c. test by extrapolating the results back to one loading cycle was less than a factor of two higher than the value measured in the tensile test. However, physical differences between the tests include: thermomechanical vs mechanical stressing; elevated and variable temperature in the a.c. test; residual stresses in the film on substrate vs none in the free-standing tensile specimen; substrate constraint causing biaxial loading as well as additional strengthening in the a.c. test; and cyclic loading vs monotonic strain to failure. By more realistic treatment of these differences, in measurements on specimens of different materials with different grain sizes and different line widths, we will quantify the uncertainty with which static mechanical properties can be deduced from the a.c. test. By comparison, the rule for obtaining the ultimate tensile strength from a nanoindentation test typically overestimates the microtensile result by a similar amount.

DELIVERABLES: We are planning the 2nd NIST Workshop on Reliability Issues in Nanomaterials. 3Q 2007

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

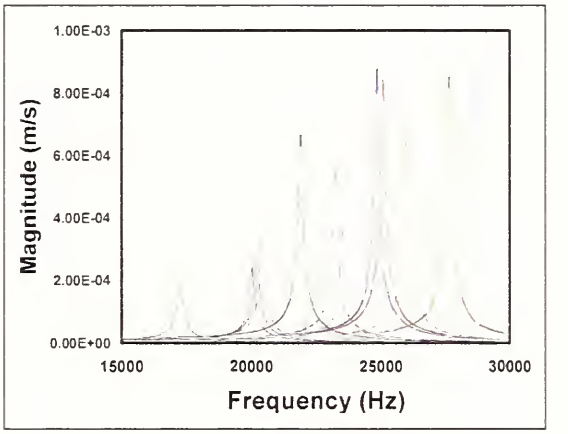

Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams and measurements of residual strain and strain gradient can be made. With the residual strains, from the fixed-fixed beam method, the elastic constant, from the resonant method, and the strain gradient, from the curvature of cantilevers, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens. 4Q 2006

Accomplishments

■ Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Currently we are placing major focus on the comparison of stress-to-failure a.c. electrical tests vs. microtensile tests. Figure 3 shows the effect of line width on current density at failure in ramp-to-failure tests. Such scale-related effects will have to be factored into analysis procedures for deducing material properties from a.c. tests.

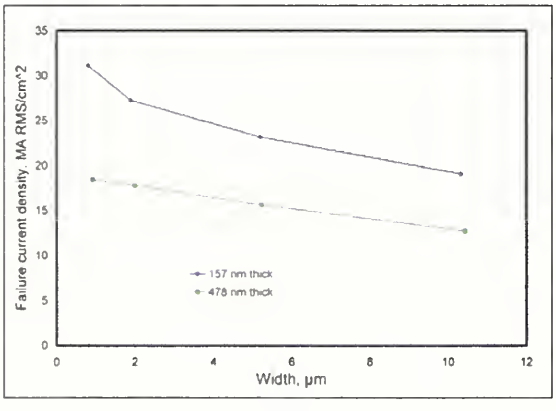

Figure 3. Effect of line width on current density at failure in ramp-to-failure tests in PVD copper films.

■ Based on input received at the workshop on Reliability Issues in Nanomaterials, discussed above, an international round robin to assess interlaboratory reproducibility of measurements of hardness and elastic modulus by instrumented indentation, on thin film materials typical of those used in interconnect structures in microelectronic devices, has been conducted; a technical publication reporting the results is in review.

DELIVERABLES: Paper reporting round robin is in review for a special issue of a technical journal. 2Q 2006

■ A specimen film selected after consultation with a group of experts in the field, consisting of a copper film with a platinum passivation layer, was contributed by Sandia National Laboratory. Open participation was solicited by e-mail to over 100 laboratories. Fragments of the specimen wafer were distributed to approximately 30 laboratories around the world. The goal was to obtain results representative of the experience of a "typical customer" using a testing laboratory. Approximately 25 laboratories conducted tests and contributed reports. The results have been analyzed with assistance from the NIST Statistical Engineering Division. The scatter in modulus and hardness are much larger from laboratory to laboratory than within laboratories; Fig. 4 shows the hardness data.

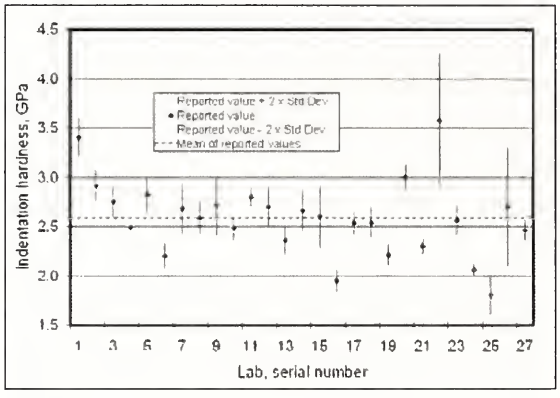
Indentation hardness, GPa
Lab, serial number
Reported value + 2 x Std Dev
Reported value
Reported value - 2 x Std Dev
Mean of reported values

Figure 4. Reported results for indentation hardness of the round robin specimen material, a Cu film on a silicon substrate. The error bars at each data point span a total range of 4 times the standard deviation reported for multiple indentations. The average of the reported hardness values is 2.59 GPa.

This result indicates that comparisons of instrumented indentation results from different laboratories should be treated with caution, and that further investigation is needed to identify the sources of the scatter.

DELIVERABLES: Papers based on three conference presentations on the comparison of electrical and mechanical stress effects are in review for the respective technical conference proceedings, to appear in 4Q 2006.

■ We have been working to demonstrate the applicability of our small-scale mechanical testing techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5.

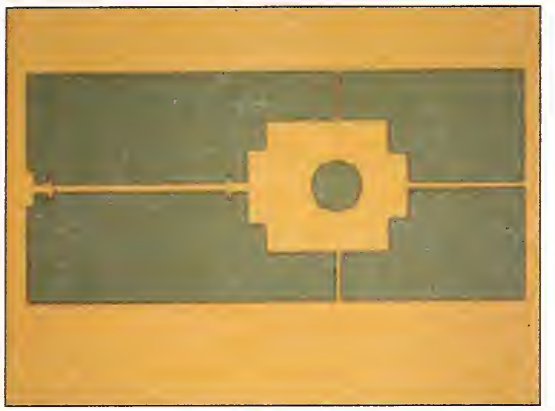

Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 μm to 10 μm, increases the ductility from around 1 % or less to 5 % or more. These data were obtained in microtensile tests of a new variety of electrodeposited copper supplied by an industry collaborator. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 °C. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

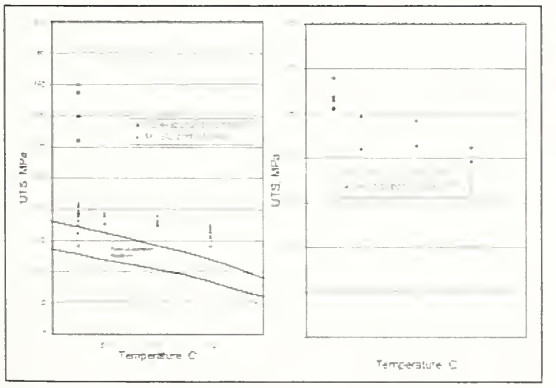

Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The atoms shown as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for

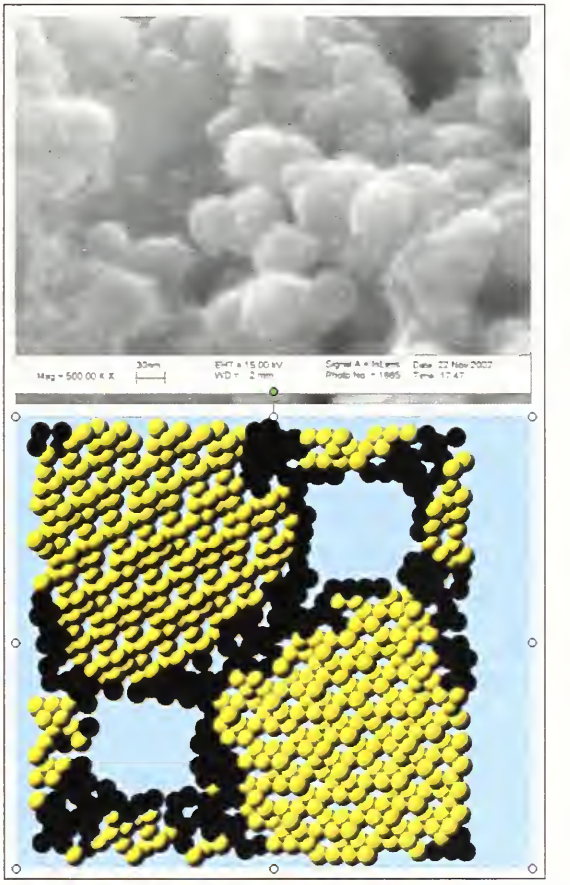

Figure 7. (a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper "balls" are 30–50 nm in diameter. (b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal face-centered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000 atom model simulates a specimen of indefinite size.

our measured values of the elastic constant of ED copper, which are lower than the bulk value. We have extended our atomistic modeling to the mechanical behavior of quantum dot structures such as germanium in silicon and indium arsenide in gallium arsenide, specifically, the strain in and around the heterogeneous inclusion. Strains surrounding the quantum dot structures play an important role in creating the confined electron states and in providing a driving force for self-assembly of arrays of dots.

■ Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. Figure 8 shows the large difference in lifetime seen under the a.c. and d.c. test conditions. We have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 9). Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles

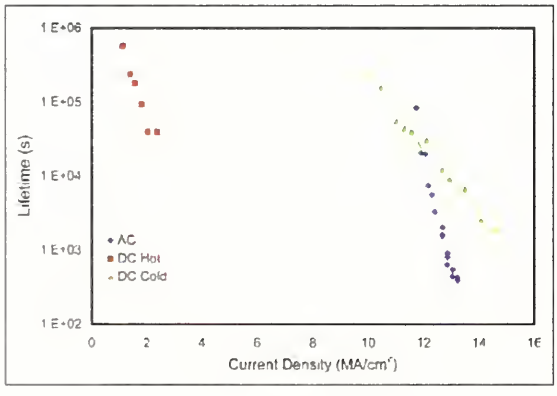

Figure 8. Time to open circuit under various electrical testing conditions. "A.C." and "D.C. Cold" data obtained with specimen nominally at room temperature. "D.C. Hot" tested at nominal specimen temperature of 227 °C. "D.C. Hot" data from U. E. Möckl, M. Bauer, O. Kraft, J. E. Sanchez, Jr., and E. Artz, MRS Symp. Proc. Vol. 338, 373 (1994).

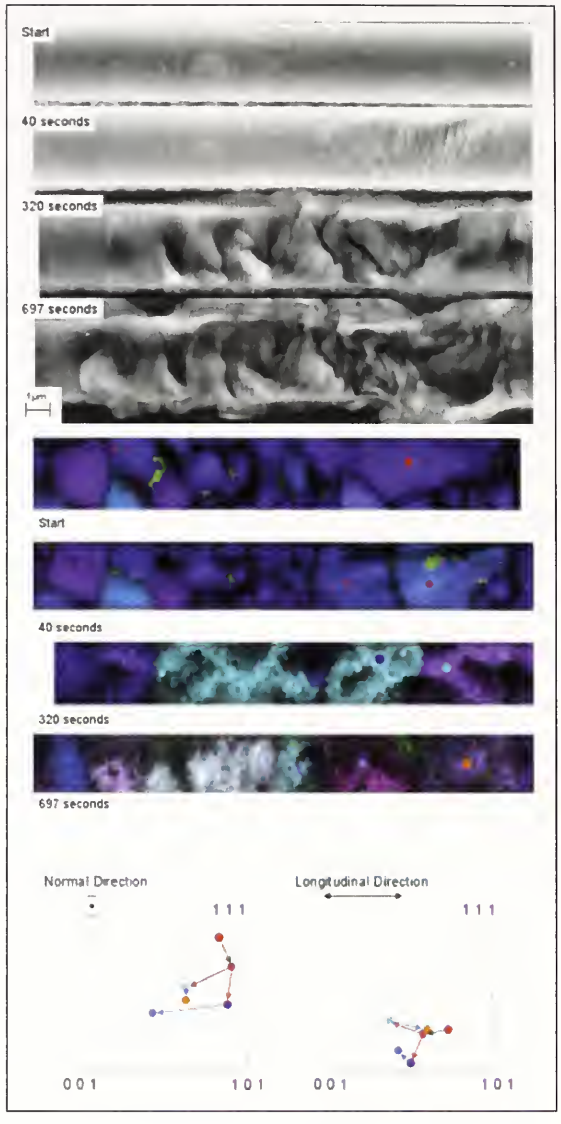

Figure 9. A.C. testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of A.C. cycling at about 12 MA/cm². Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

It is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process. In the Micro- and Nano-Electro-Mechanical Technology (MNT) Metrology Proj-

ect, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. More information on this effort can be found on that project's report.

Collaborations

Glenn Alers, Novellus Inc.

Michael Lane, IBM, Yorktown Heights, NY

Ju-Young Kim, Seoul National University, Korea

University of Karlsruhe, Germany, Prof. Eduard Arzt, Dr. Cynthia Volkert

Intel Corp., Hillsboro, OR, Dr. Brad Sun

Motorola, Inc., AISL, Tempe, AZ, Betty Yeung, and MATC, Schaumburg, IL, Dr. Andrew Skipor

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

Recent Publications

N. Barbosa III, R. R. Keller, D. T. Read, R. H. Geiss, and R. P. Vinci, *"Comparison of Electrical and Microtensile Evaluation of Mechanical Properties of an Aluminum Film,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

D. T. Read and A. A. Volinsky, *"Thin Films for Microelectronics and Photonics: Physics, Mechanics, Characterization, and Reliability,"* in Micro- and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, edited by E. Suhir, C.P. Wong, Y.C. Lee, Springer, New York, 2006.

D. T. Read, R. R. Keller, N. Barbosa III, and R. H. Geiss, *"Nanoindentation Round Robin on Thin Film Copper on Silicon,"* submitted to Metallurgical and Materials Transactions April 2006. Paper presented at 2006 TMS Annual Meeting.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, *"Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects,"* Mater. Res. Soc. Symp. Proc. Vol. 863, B9.5.1, (2005).

R. H. Geiss, R. R. Keller, D. T. Read, and Y.-W. Cheng, *"TEM-Based Analysis of Defects Induced by A.C. Thermomechanical versus Microtensile Deformation in Aluminum Thin Films,"* Mater. Res. Soc. Symp. Proc. Vol. 863, B7.2.1, (2005).

R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, *"Electrical Methods for Mechanical Characterization of Interconnect Thin Films,"* 2005 Advanced Metallization Conference.

R. H. Geiss, D. T. Read, A. Roshko, K. A. Bertness, and R. R. Keller, *"Applications of EBSD to the Study of Localized Deformation,"* 2005 Microscopy and Microanalysis Meeting.

Robert R. Keller, David T. Read, and Roop Mahajan, NIST Special Publication 1043, Workshop on Reliability Issues in Nanomaterials, U.S. Department of Commerce, August 2005.

R. R. Keller, and D. T. Read, *"The NIST Workshop on Reliability Issues in Nanomaterials, August 17-19, 2004,"* Proceedings, Government Microcircuit Applications & Critical Technology Conference 2005, Las Vegas, NV, April 4-7, 2005.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, *"Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects,"* Materials, Technology, and Reliability of Advanced Interconnects: MRS Symposium Proceedings, March 28-April 4, 2005, San Francisco, CA.

R. H. Geiss, R. R. Keller, D. T. Read, and Y.-W. Cheng, *"TEM Analysis of Deformation in Thin Films of Aluminum after both A.C. Thermomechanical and Tensile Deformation,"* Thin Films – Stresses and Mechanical Properties XI: MRS Symposium Proceedings, March 28-April 4, 2005, San Francisco, CA.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, "Electric Current Induced Thermomechanical Fatigue Testing of Interconnects," AIP Conference Proceedings 788, Characterization and Metrology for ULSI Technology, pp. 491-495 (2005).

Y.-W. Cheng, D. T. Read, J. D. McColskey, J. E. Wright, *"A tensile-testing technique for micrometer-sized free-standing thin films,"* Thin Solid Films 484 (1-2), 426-432, 2005.

D. T. Read, *"Atomistic simulation of modulus deficit in an aggregate of metal spheres,"* Journal of Applied Physics 97 (1): Art. No. 013522, January 1, 2005.

R. R. Keller, R. H. Geiss, Y.-W. Cheng, and D. T. Read, *"Microstructure Evolution During Alternating-Current-Induced Fatigue,"* IMECE2004-61291, Proceedings of IMECE04, 2004 ASME International Mechanical Engineering Congress and Exposition, November 13-20, 2004.

D. T. Read, Y.-W. Cheng, and R. Geiss, *"Mechanical Behavior of Electrodeposited Copper Film at Elevated Temperatures,"* IMECE2004-61320, Proceedings of IMECE04, 2004 ASME International Mechanical Engineering Congress and Exposition, November 13-20, 2004.

R. Monig, R. R. Keller, and C. A. Volkert, *"Thermal fatigue testing of thin metal films,"* Review of Scientific Instruments 75 (11): 4997-5004, November 2004.

D. T. Read, Y.-W. Cheng, and R. Geiss, "Morphology, Microstructure, and Mechanical Properties of a Copper Electrodeposit," Microelectronic Engineering, 75 (1): 63-70, July, 2004.

D. Josell, C. Burkhard, Y. Li, Y.-W. Cheng, R. R. Keller, C. A. Witt, D. R. Kelley, J. E. Bonevich, B. C. Baker, B. C., and P. Moffat, "Electrical properties of superfilled sub-micrometer silver metallizations," Journal of Applied Physics, 96 (1): 759-768, July 1, 2004.

Test Structures For Interconnect Metrology and Modeling

Technical Contacts:
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H. Schafft

Goals

The overall goal is to make contributions to a test-structure infrastructure that is relevant to selected state-of-the-art interconnect-system needs as stated by the ITRS *Interconnect* Report 2005 which states that the function of an interconnect system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of integrated circuits in the face of further scaling of feature sizes.

Test-structure metrology applications can be classified into two categories: (1) optimal selection of materials and processes for developing and maintaining fabrication processes for new interconnect systems that comply with increasing device density and performance needs, and, (2) parameter extraction for modeling and predicting the performance of interconnect systems for particular fabrication architectures. In the first category, the project's test structures for process development target the extraction, by electrical means, of key dimensional parameters such as conducting-feature CD. This is a key unsolved problem for cases in which copper conductors are embedded in barrier metals of different species. Additionally, the adverse interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features, particularly those of the wider upper-level conductors, is a related and as-yet unresolved issue. In the second category, a near-term goal in materials studies is the fabrication of electrically testable, all copper, features having lateral dimensions in the 20- to 100 nm range. This project's unique approach seeks to assess the impact of CD sealing on the fundamental physics of electron transport in features built from single metal species, such as copper, without the metrology complications resulting from having other metal species incorporated into interconnect features. The information is to generate a computational infrastructure to facilitate modeling the performance of features that are replicated with two or more metals and to aid the verification of dimensional parameter extraction for process-control purposes. Among the test structures being implemented for modeling the performance of advanced interconnect implementations are strip lines that are to be rf-tested from d.c. to 10 GHz, consistent with projected clock speeds of integrated circuits over the next half decade.

Customer Needs

Interconnect is becoming the principal factor that determines the maximum performance that can be attained with emerging generations of integrated circuits. The dramatic reversal from performance which is limited by transistor delay, to performance which is limited by interconnect delay, challenges the approach of continuing to scale the conventional metal/dielectric system to meet future interconnect requirements. Future advances in IC performance will be governed increasingly by the advances in interconnect technology, at least as much as by advances in active devices. As aluminum is replaced by hybrid copper/barrier-metal conductors, the initial benefits of the higher conductivity are becoming problematic as a result of the predominance of contributions of the barrier metal to the effective conductor resistance. There are two mechanisms. When barrier metal, with its higher resistivity, replaces more highly conducting copper, the proportion of the total CD, which is allocated to copper, is reduced dramatically as CD is scaled. Confounding the phenomenon, higher clock speeds favor conduction by the outer regions of the composite conductor, which render it adversely non-linear. Modeling the generalized binary-metal interconnect conductors at high frequencies is therefore a central issue. This is a very complex task on which no known reports exist in the technical literature. However, we have been able to make a start on providing a tool for dealing with this issue by drawing on NIST resources in other Divisions.

Whereas there is no simple global solution to the challenge of electrical metrology for the extracting the CDs of binary-metal interconnect conductors at this time, advances being pursued by this project are likely to play a leading role. Finally, a metrology challenge that is attributable as much to scaling per se, rather than to the materials selected for interconnect implementation, is overlay. Overlay metrology is being challenged by exacerbation of the tool- and wafer-induced shifts that are generally manageable for technology generations introduced prior to the present time.

Technical Strategy

The four-part current technical strategy is to build on opportunities afforded by the project's unique SCCDRM experience. The same substrates that have been developed for CD reference-material applications are being applied to the fabrication of single-metal, initially copper-only, test structures with features having lateral dimensions in the 20- to 100 nm range. The novel process-flow, which has been reported in a joint paper with the University of Edinburgh at a recent conference, is illustrated in Fig. 1. The approach shown there enables a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the complications resulting from having other metal species that serve as barrier layers. The information so provided enables modeling the performance of features that are replicated with copper-cored binary-metal technology and will aid in the verification of dimensional parameter extraction for process-control purposes.

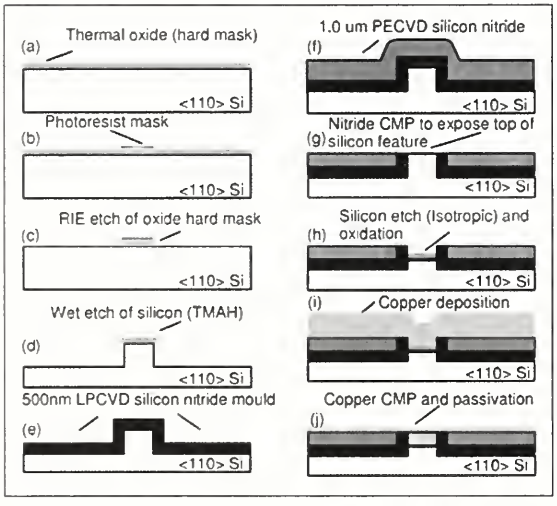

Figure 1. The process flow which was devised for the fabrication of single-metal, copper-only, test structures with features having lateral dimensions in the 20- to 100 nm range.

The project's tool-kit has a test structure that will allow the extraction, by electrical means, of key dimensional parameters for process-control purposes such as copper-cored interconnect feature CD. This responds to an unsolved problem when copper conductors are embedded in barrier metals. The solution is sought after by companies marketing interconnect-system modeling software tools and their industry clients. Our strategy is based on a test structure we first proposed and published several years ago.

We are initiating a study of the interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features at frequencies that need to be extended to ~100 GHz. This higher upper limit is driven by near-term year clock speeds having rising and falling edge components that substantially exceed 20 GHz. As mentioned above, higher clock speeds favor conduction by the outer regions of the binary-metal interconnect conductor through the so-called "skin effect" phenomenon, which render it adversely non-linear. The technical strategy is to model the RLGC parameters of a selection of binary-metal interconnect-conductor architectures over the stated range of frequencies using finite-element Maxwell software, which is available at NIST. This approach is quite ambitious and there are no known analytical solutions for generalized binary-metal interconnect conductors. Since there is no report of such analyses in the scientific literature, we have chosen first to verify our Maxwell solutions for a selection of single-metal architectures for which analytical solutions do exist.

A class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. This project has successfully applied for a patent on an electrically calibrated test structure to serve as a process- and tool-specific overlay standard that avoids all the limitations of other approaches. The strategy is to reduce the concept to practice by replicating the test structures with a bi-level polysilicon-metal process and conduct parametrical testing. Among the test structures that are being designed for modeling-parameter extraction are strip lines that will be rf-tested from d.c. to 40 GHz, consistent with clock speeds of road-map integrated circuits over the next several years. The strategy is the computation of rf-impedance parameters from S-parameter measurements. An important spin-off from this activity is the application of rf-measurement to validating key dimensional parameters of masks which are patterned for interconnect fabrication, another application which has been sought by the mask-vendor and mask-user industries. This work will be done initially on binary masks but, if successful, will be extended to the examination of opportunities in dimensional metrology for more complex binary-mask applications. Further into the future, the experience gained here may be useful for development of a non-contact electrical-CD metrology, which is understood to be needed by the photo-mask industry.

The ITRS *Interconnect* Report of 2005 relates how both grain-size and feature dimensions affect the effective resistivity of copper in the electrical wiring of integrated circuits. The consequences are of growing concern because new technologies require ever-smaller dimensions that lead to greater resistance and faster operation, which requires smaller resistance. This project strategy is to develop an easy-to-use, versatile effective-resistivity simulation program that is superior to other approaches in use for studying size effects in collaboration with a graduate program at George Washington University. It shows how scattering of electrons by surfaces, grain boundaries, and impurities increases the effective resistivity of copper in thin films and lines as dimensions approach and become shorter than the mean free path of electrons in bulk copper. In related experimental work, is copper films are fabricated, their sheet resistances and physical thicknesses are measured, and the predictions of the simulation program are compared to experimental results. Figure 2 shows the various scattering events that are included in the simulation program to simulate size effects in copper that was reported in a recent NIST news release.

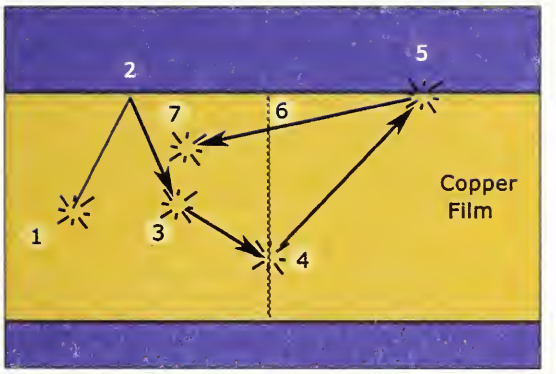

Figure 2. The scattering events that are included in the simulation program to simulate dimensional effects in copper.

The project is also providing technical and related support to the JEDEC Committee JC14.2 on Wafer Level Reliability of the JEDEC Solid State Technology Association to enhance the reliability of in the new copper interconnect technologies. This support is for revising interconnect standards, which were originally written for aluminum interconnects, so that they will be applicable to copper metallization. The primary focus is in writing a new JEDEC standard for constant current and temperature stress testing for electromigration, assisting in revising the JEDEC standard for isothermal stress testing for electromigration, assisting in preparing a new JEDEC stress test for stress voiding, and for preparing JEDEC guidelines for designing stress-voiding test structures.

DELIVERABLES:

- Report results of modeling the distributed resistance values of interconnect conductors that can be simulated by both analytical solutions and a commercial Maxwell solver. 1Q 2007
- Complete analysis of experimental measured increase in effective resistivity of copper films with thicknesses decreasing from approximately 200 nm to 15 nm, and compare measurements with simulation results. 3Q 2006
- Complete for publication a new JEDEC standard for electro-migration stress testing with constant current and temperature. 1Q 2006
- Design, and verify by simulation, the performance of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication. 3Q 2006
- Fabricate and test chemically stable test structures having copper-only features and make ECD measurements. 4Q 2006
- Report initial electrical measurements made on second-generation SCCDRM test structures that have been converted to single-crystal nickel-silicide. 1Q 2007
- Design, model, fabricate, and test a selection of co-planar waveguide test structures on chrome-on-glass photo-masks to evaluate the efficacy of developing a non-contact ECD method for sampling printed features. 4Q 2006

Accomplishments

■ As a result of close extended collaboration with the University of Edinburgh, the project has been able to develop and report a unique copper damascene process for the fabrication of a scaled electrical test structure having copper-only features. The purpose is to facilitate studies of electron transport in pure copper without having to correct for the complexities of the interaction of copper with barrier-metal films. This implementation enables the separation of the effects of surface and grain-boundary scattering, as a function of the cross-section dimensions of the conductor by electrical testing. A joint paper describing the accomplishment was presented at the ICMTS 2006 conference in Austin, Texas, on March 8, 2006.

■ In close collaboration with NIST operations in Boulder, Colorado, Maxwell software was applied to the calculation of RGLC parameters of cylindrical copper conductors with diameters ranging from 50 nm to 5000 nm, which were coated with TaN barrier metal of thicknesses typical of current IC-interconnect applications. At frequencies above 10 GHz, significant increases in resistance were observed. These results have been set aside to allow for verification of the modeling by comparing those of a selection for copper-only wires that were obtained from exact solutions based on Maxwell's equations. Initial results indicate close comparisons for the cases that have so far been compared.

■ A paper that describes a new simulation program and its use to study the effects of surface and grain-boundary scattering on the effective resistivity of copper in thin planar films and small cross-section lines was completed. The paper was accepted for publication by the Microelectronics Reliability journal for appearance in mid-2006.

■ A report was completed that describes a computer program, which simulates the impact of the size on the effective resistivity of line and film conductors. Flow charts and the program code are provided as appendices. This work was published in February 2006 as an NISTIR.

■ In close collaboration with the Laboratory for Interconnect and packaging at the University of Texas at Austin, test structures for the investigation of the effect of linewidth scaling on electron transport in nickel mono-silicide features have been designed and fabricated. The features were patterned on (110) silicon-on-insulator wafers with i-line lithography that replicated test structures from which voltage/current (V/I) measurements could be extracted. Subsequently, the patterning of single-crystal features with direct-write electron-beam lithography has been developed in order to facilitate the future reduction of the linewidths of NiSi features having a highly controlled surface microstructure to linewidths below 40 nm. Figure 3 shows a selection of 40 nm features that were etched in (110) silicon after electron-beam lithography as reported in a joint paper with the University of Texas at Austin at a recent conference.

■ Work has been initiated on a new CD metrology based on coplanar waveguide test structures. Extensive e-m field modeling of characteristic impedance and distributed capacitance, which we have conducted in collaboration with the Department of Electrical & Computer Engineering at George Washington University, indicates that the extraction of these values from s-parameter measurements can be applied to sampling CDs of test-structure features that are printed on photomasks. At this time, the design of a set of thru and de-embedding structures has been designed and a supplier of the substrate has been identified.

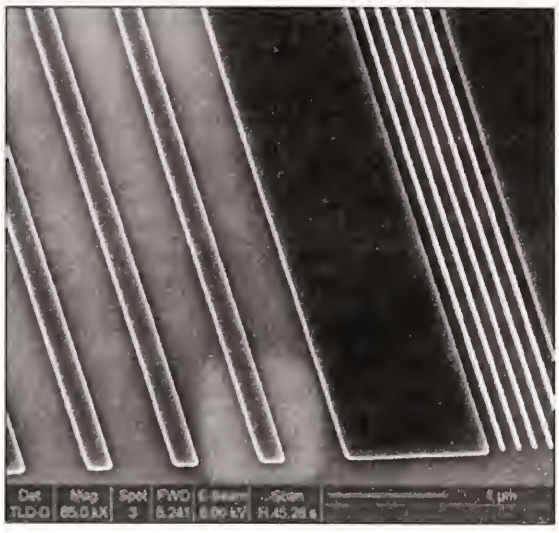

Figure 3. A selection of 40 nm features that were etched in (110) silicon after electron-beam lithography.

■ A poster paper was delivered at the 2005 IEEE International Integrated Reliability Workshop to discuss the details of the model used to simulate size effect on the resistivity of copper, and to describe results of the simulation studies.

■ A new JEDEC standard JESD202 was completed and published in March 2006. The standard describes an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a lognormal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Procedures are provided to analyze complete and singly, right-censored failure-time data.

■ The CAD of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication has been completed. A program to simulate and validate the calibration of the standard has been applied to the design and fabrication of a wafer-lot has been initiated.

Collaborations

The leading collaborators are semiconductor processing facilities and laboratories at three major Universities.

The Scottish Microelectronics Centre at the University of Edinburgh (SMC) is now providing a substantial part of the project's wafer fabrication operations. More importantly, the staff there are highly and broadly experienced in interconnect fabrication materials, processes, and issues. Audio teleconferences are exchanged between Project and SMC staff on this and a second project regularly.

The Electrical-Engineering and Computer-Sciences Department at George Washington University has been funding the studies of Ph.D students and a Professor to work on this NIST Project for almost a decade. The present collaboration contributes special skills in rf parameter extraction and the physics of electron transport.

A new collaboration with the Department at the University of Texas at Austin has resulted on the transformation of narrow SCCDRM features to silicide material. They are also contributing very desirable ultra-narrow-line lithography for the next-generation SCCDRM fabrication.

This project has always benefited from an active collaboration with Litho-Metrology Operations at SEMATECH. Although this project's focus has only recently shifted away from litho-metrology to interconnect, we are actively pursuing a parallel shift in our collaboration.

Recent Publications

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, "Implementation of Simulation Program for Modeling the Effective Resistivity of Nanometer Scale Film and Line Interconnects," NISTIR 7234, February, 2006.

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W. F. Guthrie, R. G. Dixson, R. A. Allen, M. W. Cresswell, C. E. Murabito, B. Park, "Establishing Traceability of Linewidth Reference Materials Using CD-AFM and HRTEM," 2005 International Conference on Characterization and Metrology for ULSI Technology, March 15-18, 2005, University of Texas at Dallas.

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Allen, R. A., Hunt, A. , Murabito, C. E., Park, B. , Guthrie, W. F., Cresswell, M. W., "Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging ICMTS IEEE International Conference on Microelectronic Test Structures," Leuven, Belgium April 18, 2005.

Bin Li, Li Shi, JiPing Zhou, Paul S. Ho, Richard A. Allen, Michael W. Cresswell, "Test Structures for Study of Electron Transport in Nickel Silicide Features with Linewidths between 40 nm and 160 nm," ICMTS IEEE International Conference on Microelectronic Test Structures Leuven, Belgium April 18, 2005.

CD-AFM reference metrology at NIST and SEMATECH Ronald Dixson, Joseph Fu, Ndubuisi Orji, William Guthrie, Richard Allen, and Michael Cresswell Proceedings of SPIE – Volume 5752 "Metrology, Inspection, and Process Control for Microlithography XIX," Richard M. Silver, Editor, May 2005, pp. 324-336.

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Solders and Solderability Measurements for Microelectronics

Goals

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free (Pb-free) solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

Customer Needs

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pb-free solders has been specified in the 2002 and 2004 iNEMI, 2003 and 2004–2005 IPC, and 2003 and 2005 ITRS Roadmaps. The European Community (EC) directives on Waste Electrical and Electronic Equipment (WEEE) and the Restriction of the Use of Certain Hazardous Substances (RoHS) in Electrical and Electronic Equipment take effect in July 2006. U.S. manufacturers must comply with these requirements in order to compete in the global market. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the International Electronics Manufacturing Initiative (iNEMI) technology working group (TWG) on tin (Sn) Whiskers. The protective layer of Sn deposited on copper (Cu) is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure Sn tend to grow "whiskers," however, which can cause shorts across leads (see Fig. 1). Thus the development of Pb-free Sn alloy platings to replace Pb-containing Sn layers is considered important, and tests which ascertain the tendency to form whiskers are much needed.

A series of industry sponsored workshops have been held over the past four years to address the problem of Sn whisker growth that has arisen due to worldwide conversion to Pb-free solder technology. These workshops have reached the consensus that residual compressive stress in the tin is the basic cause of whisker growth. The international organization representing these industries and organizing the workshops, iNEMI, has asked the Metallurgy Division (via a letter to F. Gayle, 10/14/2005) to focus on the, "Establishment of Primary and Secondary Standards for $\sin^2\Psi$ stress determination in electroplated tin films and to write a measurement technique standard for tin film $\sin^2\Psi$." Further they ask NIST to, ".... take the leadership role in developing the measurement standards and the required degree of process specificity."

Technical Strategy

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. For example, a special NIST publication, "Recommended Practice Guide for Differential Thermal Analysis (DTA) and Heat Flux Differential Thermal Analysis (DSC) Measurements of Alloy Melting and Freezing" will

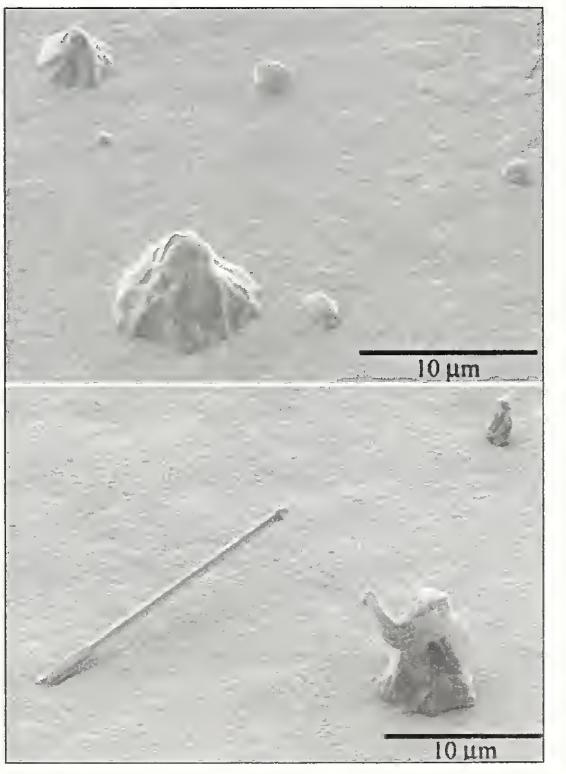

Figure 1. Top) Sn hillocks grew on the surface of pure Sn deposit. Bottom) Sn whiskers and contorted Sn hillocks grew on the surface of Sn-Cu alloy deposit. These surface disturbances formed even though W was used as a substrate for plating, which does not form an intermetallic compound with Sn.

Technical Contacts:
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U. Kattner
K. W. Moon
M. Williams

"I consider your [NIST Metallurgy Division] group a key asset to industry in making these decisions on the soundest possible scientific basis. There is no comparable body of expertise anywhere in the world that matches that found in your group."

Dr. George T. Galyon (IBM)
-Chairman, NEMI Tin Whisker Modeling Committee

give researchers a consistent method to interpret thermal analysis data of solders and other alloys. In addition, a thermodynamic database has been developed and publicly distributed for modeling the processing behavior of Pb-free solder systems. These databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will continue to be expanded and distributed via the web. We also provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (filamentary whiskers typically 1 μm diameter and several mm long) can grow from the plating and cause electrical shorts and failure. Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program. it was decided to focus on Pb-free Sn-rich deposits with alloying additions that might retard whisker formation. The Sn-Cu system was selected for compatibility reasons, since Sn-Cu-Ag is likely to be the Pb-free solder of choice for industrial application. The substitution of a different solute for Pb in the Sn-rich deposit was proposed to also retard whisker growth. A detailed microstructural comparison of deposits with high and low whisker formation tendency has been conducted. Sn grain size, shape, and residual stress have been measured and correlated to whisker growth.

DELIVERABLES:

- Determine methods to eliminate columnar grain structure in Sn electrodeposits. 3Q 2007
- Complete Manuscript "Examination of Sn Electrodeposit on Substrates Not Forming Intermetallic Compounds" to determine whisker tendency on tungsten (W) substrates that do not form intermetallic with Sn. 3Q 2006
- Determine feasibility of X-ray $\sin^2\Psi$ methods for measuring residual stress in Sn electrodeposits. 3Q 2007

Accomplishments

■ "Recommended Practice Guide for Differential Thermal Analysis (DTA) and Heat Flux Differential Thermal Analysis (DSC) Measurements of Alloy Melting and Freezing" has been completed and will appear as a NIST Special Publication Series 960. This document provides a detailed description of proper technique and measurement pitfalls in the determination of alloy liquidus and solidus temperatures; *i.e.*, the freezing (or pasty) range. Such methods are important for the selection of Pb-free solder alloys that satisfy industry specifications.

■ NIST remains a co-chair of the iNEMI Sn Whisker Modeling Group (includes members ChipPAC, Cookson, Delphi Delco, Freescale, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics). NIST is also an active participant in the iNEMI Accelerated Sn Whisker Test Group.

■ Building on the work from the recently published paper, Acta Materialia 53(2005) 5033–5050, entitled, "Hillock and Whisker Formation in Sn, Sn-Cu and Sn-Pb Electrodeposits," three new experimental studies are underway. The first two, in their early stages, focus on attempts to alter the columnar grain structure using pulse plating and/or addition of Bi which may poison the crystal growth and cause renucleation of Sn grains during the electrodeposition process. The third study focuses on the role of the reaction between the Sn and the substrate (typically Cu) to form intermetallic compound as a contributing source of residual stress. Bright Sn and bright Sn-Cu alloy were plated on Tungsten (W), a substrate material that does not form intermetallic compounds with Sn, and stored at room temperature. As with the electrodeposits on Cu, the deposits on W showed hillocks on pure Sn deposits and whiskers on Sn-Cu alloy. Thus changing the substrate had little discernable effect on the whisker defect formation.

Collaborations

International Electronics Manufacturing Initiative (iNEMI); Co-Chair of the Sn Whisker Modeling Group and a member of the Accelerated Sn Whisker Test Group. In particular extensive discussions with Dr. George Galyon, Poughkeepsie/IBM on the fundamental causes of whisker growth.

Northrup-Grumman, Linthicum, MD, Provided samples consisting of Sn-Cu electrodeposits on Zn substrates for their tests on the use of acrylic conformal coatings to prevent whisker growth.

Recent Publications

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Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Gas Property Data and Flow Standards for Improved Gas Delivery Systems

Goals

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition and the calibration of mass flow controllers (MFCs). As the data are acquired, they will be posted to an online database.

NIST also will develop primary standards for gas flow in the range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry (10^{-6} mol/s ≈1.3 standard cubic centimeters per minute (sccm)).

Customer Needs

The 2005 *International Technology Roadmap for Semiconductors* (ITRS) emphasizes that the grand challenge for front-end processes is "material limited device scaling." The Modeling and Simulations section reinforces this theme: *"Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases ... are needed."* Meeting this challenge will require improvements in MFCs for the deposition and etching of diverse new materials. Thermal MFCs meter a wide variety of toxic, flammable, and corrosive gases over a large range of flow rates. Elements necessary for improved MFCs will be accurate models of gas properties and reliable physical standards for gas flow.

Participants at an industry workshop at NIST identified the gases and properties of highest priority, and they recommended publishing the property values in a public, Web-based database. The gases include process gases, "surrogate" calibration gases, and binary mixtures of process and carrier gases. The identified properties and required uncertainties include the following.

- heat capacity at constant pressure ±0.1 %
- equation of state (gas density) ±0.1 %
- viscosity ±0.5 %
- thermal conductivity ±0.5 %

The workshop also required the following uncertainties for physical standards for gas flow.

- primary standards for gas flow ±0.025 %
- transfer standards for gas flow ±0.1 %

Technical Strategy

We are measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have relative standard uncertainties of 0.01 %. Measurement conditions range as high as 425 K and 1500 kPa (or to 80 % of the vapor pressure for condensable gases). Figure 1 shows an example of such data. The speed-of-sound data are used to determine the ideal-gas heat- capacity $C_p^0(T)$ with the targeted uncertainty of 0.1 %. The pressure and temperature-dependences of $u(T, p)$ are correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the virial equation of state for the density $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than 0.1 % for density, 10 % for viscosity, and 10 % for thermal conductivity from 200 K to 1000 K.

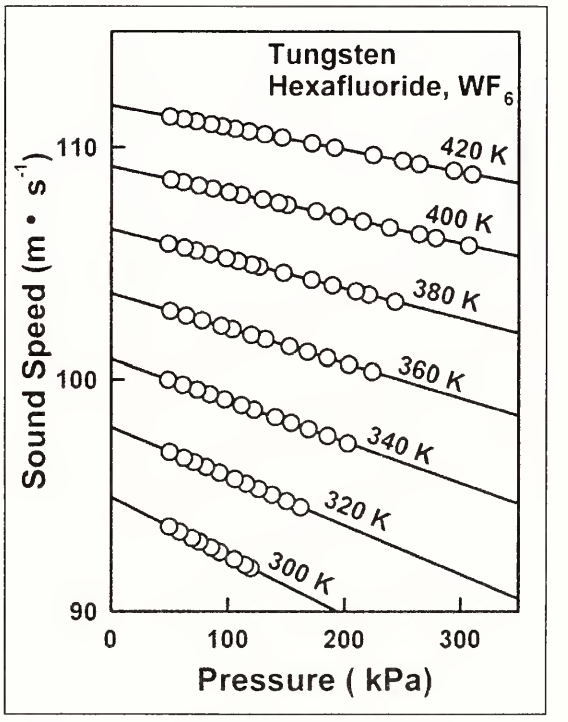

Figure 1. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

Technical Contacts:
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M. R. Moldover

"I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry. It was virtually exactly what I was searching for."

Bob Rathfelder,
Project Engineer,
Parker Hannifin

We also are developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 % as specified by the industry workshop. Figure 2 shows a second-generation acoustic viscometer made from Monel. Throughout the project, the results will be made available to industry through publications in professional journals, presentations at professional meetings, and entries in an on-line database at http://properties.nist.gov/semiprop (see Fig. 3).

Figure 2. Second-generation acoustic viscometer made from Monel for use with corrosive gases.

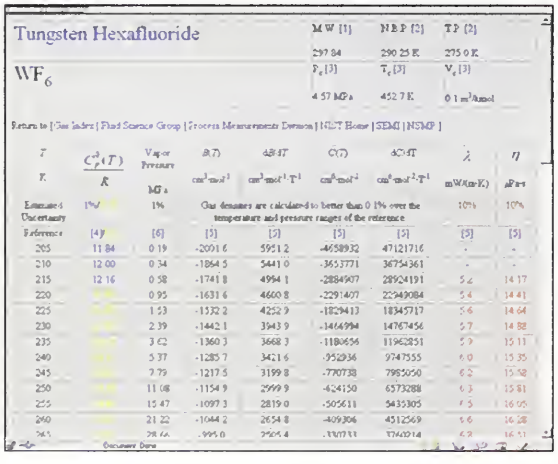

Figure 3. Sample page from on-line database located at http://properties.nist.gov/semiprop/.

We have developed a diverse series of primary standards for gas flow. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10^{-3} mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5–9 atmospheres. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle. The second and third standards have a standard uncertainty of 0.02 %. Figure 4 demonstrates the accuracy of the flow standards.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations, such as MFC manufacturers. Although a flow meter manufacturer often uses its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at fabrication facilities and MFC manufacturers. The second-generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography. It has been used for comparisons with metrological institutes of other countries as well as manufacturers of flow meters. Its standard uncertainty is 0.03 %. The third-generation standard improves convenience by combining the quartz capillary with commercial instrumentation to measure pressure and temperature.

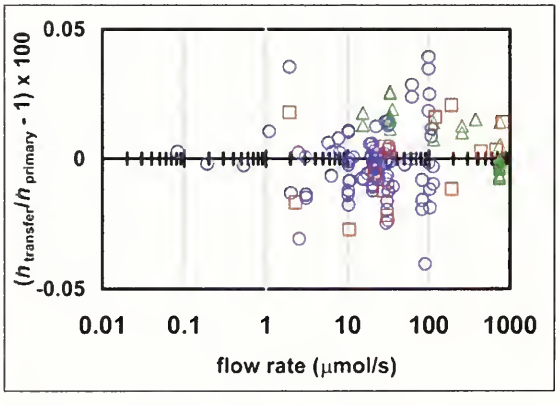

Figure 4. Comparison of three primary flow meters. The transfer standard compared the constant-pressure flow meter (circles) with the gravimetric flow meter (squares) and a constant-volume flow meter (triangles). (1 μmol/s ≈ 1.3 sccm.)

DELIVERABLES:

- Install new spherical resonator for measuring the speed of sound in the hazardous gases facility. 2Q 2006
- Calibrate resonator. 3Q 2006

A cylindrical resonator was used to study nine process gases, but it must be replaced due to contamination. A spherical resonator has been

fabricated and will be installed in the hazardous gas handling facility. The spherical resonator will be capable of producing higher accuracy measurements than the cylindrical resonator.

DELIVERABLES:

- Develop improved model of acoustic viscometer. 2Q 2006
- Develop model of acoustic thermal conductivity resonator. 3Q 2006

The second-generation Greenspan viscometer incorporates lessons learned from the previous device, thereby allowing an improved acoustic model. The model of the thermal conductivity acoustic resonator will need to be tested and further developed from calibration measurements.

DELIVERABLES: From the collected data calculate the transport properties in the semiconductor process gases identified by the customer, gases include BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. 2Q 2006

The acoustic model for the Greenspan viscometer must be applied to each data set to calculate the viscosities of the gases as a function of temperature and pressure.

DELIVERABLES: Update on-line database by 4Q 2004, publish viscosity measurements in BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. 4Q 2006

The measurements will be disseminated through papers in professional journals, talks given at professional meetings, and the on-line database.

DELIVERABLES:

- Publish in archival journal a paper on primary gas flow standards. 1Q 2006
- Repackage transfer standard based on commercial measurement package. 2Q 2006

The third-generation transfer standard will use commercial instrumentation to measure the pressures and temperature of gas flowing through a quartz capillary. The commercial instrumentation will improve the flow meter's convenience, and the quartz capillary will be similar to that of the second-generation standard. Using the same capillary and model will ensure an uncertainty of 0.1 %. An improved design based on preliminary tests will improve the reliability of the capillary package.

DELIVERABLES: Integrate static gravimetric flow standard for calibrating mole blocks. 1Q 2006

The static gravimetric flow standard is the only devices that measure directly mass flow rate instead of a secondary quantity such as velocity or heat loss. This standard is used to calibrate mole blocks as secondary standards for flows less than 1000 sccm.

DELIVERABLES: Draft SP-250 for gas flow calibrations. 4Q 2006

The SP-250 document will be used to establish a routine calibration service at NIST for gas flows in the range from 10^{-7} to 10^{-3} mol/s (1 to 1000 sccm).

Accomplishments

■ We designed and assembled a second-generation Greenspan viscometer. Its Monel construction allows the study of corrosive process gases.

■ We measured the speed of sound in the process gases Cl_2, NF_3, and N_2O. Typically, the standard uncertainty of the speed of sound was less than 0.01 %. From these data the ideal-gas heat-capacity was determined to within 0.1 %, and an equation of state was developed to predict the gas densities to within 0.1 %. Viscosity was measured in these three gases plus CF_4 and C_2F_6 with an uncertainty of approximately 0.5 %. Viscosity was also measure in the gases BCl_3, Cl_2, HBr, C_4F_8, CO, CO_2, NH_3, and SiF_4. This data set is being prepared for publication and addition to the online database.

■ We continued to provide immediate access to our results by updating the database of gas properties at http://properties.nist.gov/semiprop/.

■ We verified the accuracy of the primary flow meters by comparing the lower and upper ends of their ranges with other, overlapping NIST flow meters. Near both the lower end (0.3 sccm) and the upper end (1000 sccm) the agreement of 0.03 % was within the mutual uncertainty of the comparison.

■ We used the second-generation transfer standard and a prototype of the third-generation transfer standard to make a comparison of gas flows with a manufacturer of mass flow controllers.

Recent Publications

R. F. Berg, "Simple flow meter and viscometer of high accuracy for gases," Metrologia, **42**, 11-23 (2005).

R. F. Berg and S. A. Tison, "Two primary standards for low flows of gases," J. Res. Natl. Inst. Stan., **109**, 435-450 (2004).

J. J. Hurly, "Viscosity and speed of sound of gaseous nitrous oxide and nitrogen trifluoride measured with a greenspan viscometer," Int. J. Thermophys, **25**, 625-641 (2004).

Low Concentration of Humidity Standards

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor (< 10^{13} molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

Customer Needs

Measurement needs and technical challenges for airborne molecular contamination (AMC) in semiconductor wafer processing spanning the next 15 years are given in the 2005 International Technology Roadmap for Semiconductors (ITRS) http://public.itrs.net/. A key measure of technological progress defined in the ITRS is yield enhancement (YE) which is the process of improving baseline yield for a given technology generation from R&D yield level to mature yield. AMC affects YE and constitutes a major impediment to wafer environment contamination control particularly for 300 mm wafer manufacturing processes. An industry expert, G. Dan Hutcheson of VLSI Research Inc., estimates that "a 1 % yield increase equates to $1M per day additional profits for a modern 300 mm fabrication line," *The Chip Insider®*. The ITRS also states "The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation ... to measure AMC at the part per trillion level ... low cost, routine monitoring may be required as devices approach molecular dimensions." Target impurity levels relevant to wafer environmental contamination control for a number of AMC including H_2O, THC, CO_2 and other AMCs in various bulk gases are given in ITRS Table 115 and quantify the measurement needs in a variety of wafer production processes. Of these impurities, water vapor is one of the most ubiquitous and difficult to eliminate. Similarly, the Semiconductor Equipment Manufacturers International (SEMI) has standards describing the production and delivery and value assignment of ultra-high purity gases for semiconductor manufacturing http://downloads.semi.org/PUBS/SEMIPUBS.NSF/webstandardsgases. These standards illustrate the stringent requirements for gas purity measurements in semiconductor processes. We also note a new emphasis (beginning with the 2004 ITRS) on epitaxial processes that use gases as source materials, including SiGe and III-V semiconductor requirements for power amplifiers and extension of physical models to III-V semiconductors.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2, page 124), serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement and

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"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar,
Air Products and Chemicals

Figure 1. NIST Low Frost-Point (humidity) Generator.

generation systems at the research and development stage as well as commercial devices.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We have constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. Experience with the system has revealed several limitations of traditional implementations, including deviations of the output from the equation generally used to predict the temperature dependence of the permeation rate.

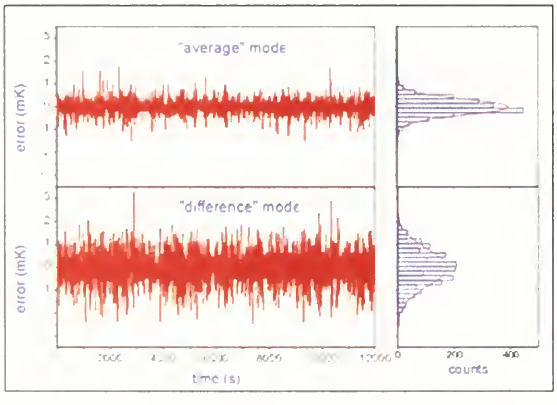

Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

DELIVERABLES:

- Complete uncertainty analysis of permeation-tube calibration system and measure temperature dependence of permeation tubes. 3Q 2006
- Complete documentation of system. 1Q 2007

2. In its standard mode of operation, the LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator. We have recently demonstrated a new strategy for pmol mol^{-1}-level humidity generation using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output stream and have validated the technique with a variety of self-consistency tests. Presently, we are establishing the uncertainties and optimal methodologies for this technique. Development of gas-handling manifolds with ultra-low adsorption/desorption of water will be a key focus of our work in the next year.

DELIVERABLES:

- Perform uncertainty analysis of dilution scheme. 3Q 2006
- Develop improved gas purification scheme for the dry-gas source. 4Q 2006
- Investigate attainable dry-drown rates using coated tubes for gas manifolds. 2Q 2007

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct vibrational absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line intensities. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high

precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method (Fig. 3). CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequeney-stabilized cavity ring-down spectroscopy (FS-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. Taking advantage of the high spectral resolution afforded by FS-CRDS, various line shape effects such as speed-dependent pressure-broadening and collisional narrowing of these transition line shapes by various media can now be quantified.

Using the existing FS-CRDS apparatus and a portable fiber-optics-based FS-CRDS system, we will make multiple independent measurements of H_2O transition line shapes and line intensities in the vicinity of 1380 nm. We will use transfer standards for humidity generation and measurement as well direct measurement of humidified gas samples delivered by the thermodynamic-based LFPG.

DELIVERABLES:

- Assemble and test portable FS-CRDS apparatus based on 1380 nm fiber-optic DFB laser for real-time continuous monitoring of LFPG output. 2Q 2006

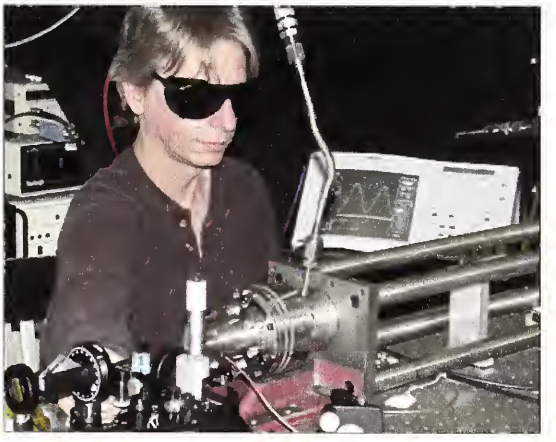

Figure 3. Frequency-stabilized CRDS system.

- Link H_2O transition line intensities in the 1380 nm spectral region to LFPG for water vapor concentration measurements in the range 1 μmol mol^{-1} to 100 μmol mol^{-1} and measure line shape effects in N_2 and other gases. 4Q 2006
- Optimize the FS-CRDS apparatus for minimum water background, and compare FS-CRDS response to diluted gas streams from the LFPG, at concentrations of 10 nmol mol^{-1}. 1Q 2007

5. Moisture contamination is a serious problem in phosphine, arsine, silane, ammonia, and similar gases used in the epitaxial growth of high-purity semiconductor layers. Semiconductor device manufacturers have expressed frustration with the irreproducibility of source material purity from vendor lot to vendor lot. The critical concentrations of the impurities are not well known; however, it is believed that >10 nmol/mol oxygen or water in most process gases is undesirable. Optical methods for measuring the moisture impurity concentrations combine high sensitivity and straight-forward traceability through the LFPG absorption line strength measurements. In collaboration with researchers in the NIST Chemical Science and Technology Laboratory, researchers in the NIST Electronics and Electrical Engineering Laboratory have developed a CRDS system linked with a semiconductor crystal growth system to measure H_2O at very low concentrations in semiconductor source gases and to correlate the process gas impurities with crystal properties. The system is being used to measure the lineshape, absorption coefficients, and frequency of optical transitions for water, phosphine, and ammonia in the vicinity of 935 nm and 1380 nm. This information is critical to facilitate the use of high-sensitivity spectroscopy techniques in these gases. The laboratory is equipped to allow safe handling of toxic gases such as phosphine and arsine, enabling collaborative experiments with industry on direct measurements of moisture in those gases. The CRDS capability should ultimately lead to improvements in semiconductor source gas purity, which will allow crystal growers to choose less expensive growth conditions without sacrificing optical emission efficiency and yield in LEDs, semiconductor lasers, and photodetectors.

DELIVERABLES:

- Modify CRDS system for parallel tests with commercial instrumentation and conduct joint experiments on H_2O in phosphine. 3Q 2005
- Measure phosphine absorption lines in vicinity of H_2O transition line at 943.082 nm and compare to previous H_2O lines explored for overlap with phosphine. If new line offers superior sensitivity, measure pressure broadening coefficients for H_2O in phosphine. 4Q 2005

Accomplishments

- We have constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and high-sensitivity quartz crystal microbalance (QCM). The water-containing permeation tubes to be calibrated are

Figure 4. New PTG calibration apparatus.

placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2. The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1 %, which is significantly superior to traditional gravimetric methods.

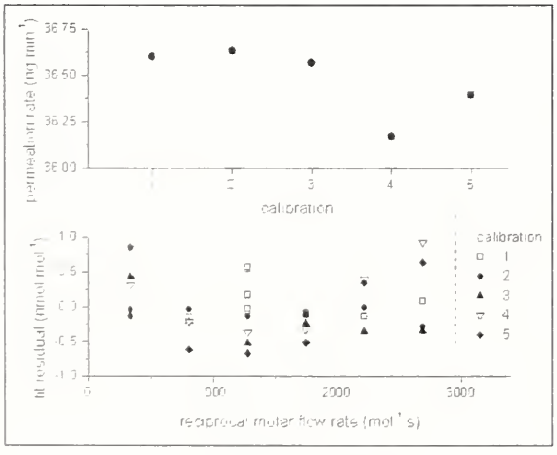

Figure 5. Calibration repeatability (top) and deviations from the fitting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

- A new strategy for pmol mol^{-1} (ppt)-level humidity generation has been successfully implemented. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above. At mole fractions below 10^{-9}, the uncertainty in water vapor mole fraction is dominated by water vapor background produced by adsorption/desorption of water on internal plumbing surfaces and by water vapor remaining in the diluent after purification. We performed three sets of measurements to validate the method. First, the same nominal output concentration was produced while varying both the water vapor concentration produced by the Low Frost-Point Generator and the level of flow dilution. Deviations from a constant concentration were measured. Second, the calculated water vapor mole fraction of the diluted generator output was compared against the reading of a commercial hygrometer based on cavity ring-down spectroscopy. Third, we measured the water remaining in the diluent gas after purification at various flow-rates both with and without an additional cryotrap. An approximate water background of 0.3×10^{-9} was inferred from the data, and the results were consistent within the combined uncertainty of the LFPG output and the water background.

- The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption

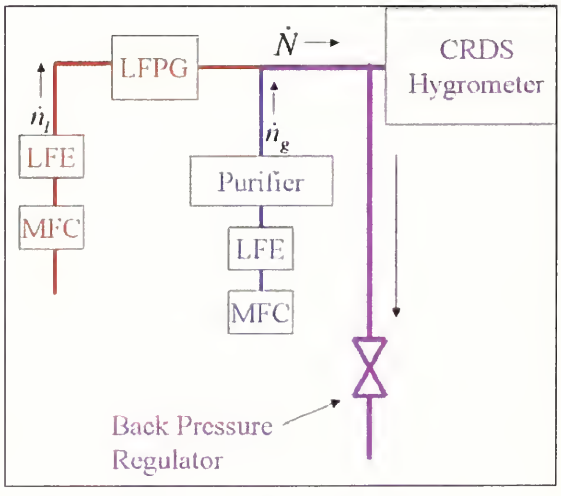

Figure 6. Dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 7, indicate that the background contribution to H_2O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1 nmol/mol.

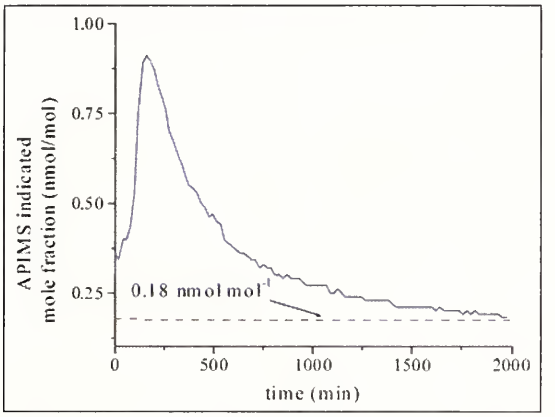

Figure 7. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

■ We have successfully developed an FS-CRDS system with automated spectral scanning capability to measure the absorption coefficient of trace quantities of water vapor. In FY 2005 the FS-CRDS method was used to probe H_2O absorption transitions in the 935 nm spectral region, and a spectral resolution of 50 kHz and reproducibility better than 0.25 % were demonstrated. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line intensities less than 0.5 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N_2 as the buffer gas). These results illustrate that the spectral resolution and linearity of the FS-CRDS method enable precise quantification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determination

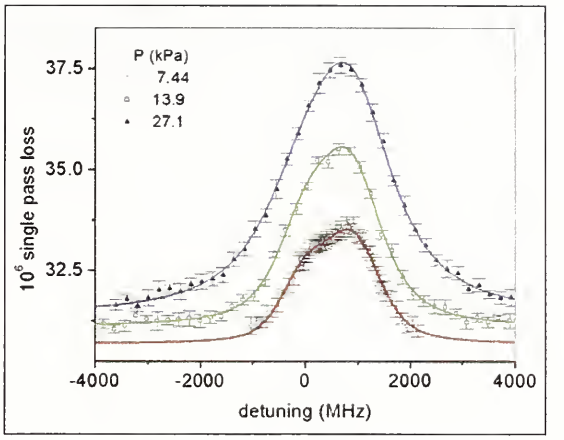

Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

of number density and line intensity that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm.

We have used a similar FS-CRDS system to measure water vapor concentrations in the toxic gas phosphine in the 935 nm spectral region. Testing of five strong water absorption lines in this region indicated that the least overlap with phosphine lines, and hence the highest sensitivity to water contamination, is present for the line at 943.082 nm. Future experiments will characterize this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 9 shows a typical H_2O spectrum obtained with the automated FSSM-CRDS system and comparison with previously published measurements.

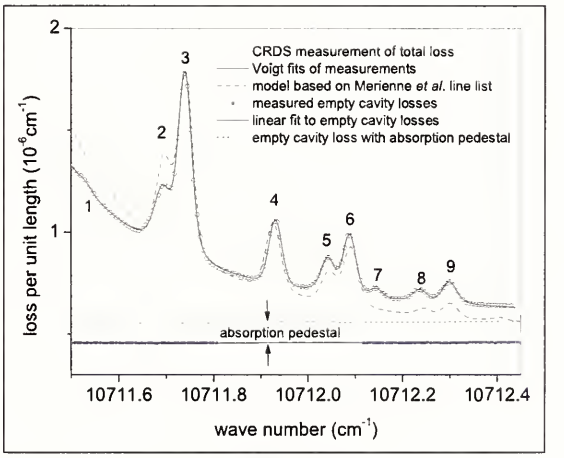

Figure 9. Survey spectrum of water vapor obtained with frequency stabilized CRDS apparatus. The numbers correspond to peaks of individual absorption transitions.

Collaborations

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

Matheson Tri-Gas, Mark Raynor and Hans Funke; CRDS measurements of trace moisture in phosphine.

Tiger Optics, Yu Chen; CRDS measurements of trace moisture in phosphine.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Tiger Optics, Calvin Krusen ; evaluation of commercial CRDS technology.

Air Products and Chemicals Inc.; CRDS measurements of trace H_2O in corrosive process gases.

Recent Publications

G. E. Scace, *"Generating Parts per Trillion Levels of Water Vapor in Nitrogen,"* in Proc. 5th International Symposium on Humidity and Moisture, Rio de Janiero, 2006 (in press).

J. T. Hodges and G. E. Scace, *"Advanced humidity standards address new demand for measurements of trace water vapor in specialty gases,"* (Micro, in press).

D. Lisak, J.T. Hodges and R. Ciurylo *"Comparison of semi-classical line shape models to rovibrational H_2O spectra measured by frequency-stabilized cavity ring-down spectroscopy,"* Phys. Rev. A., 73, 012507 (2006).

V. Vorsa, S. Dheandhanoo, S. Ketkar, and J. T. Hodges, *"Quantitative absorption spectroscopy of residual water vapor in high purity gases: Pressure-broadening of the 1.39253 μm H_2O transition by N_2, HCl, HBr, Cl_2 and O_2,"* Appl. Optics, 44, 611-619, (2005).

J. T. Hodges and R. Ciurylo, *"Automated high-resolution frequency-stabilized cavity ring-down spectrometer,"* Rev. Sci. Instrum., 76, 023112 (2005).

J. G. Cormier, J.T. Hodges, and J.R. Drummond, *"Infrared water vapor continuum absorption at atmospheric temperatures,"* Jour. Chem. Phys., 122, 114309 (2005).

S. Y. Lehmann, K. A. Bertness, and J. T. Hodges, *"Optimal spectral region for real-time monitoring of sub-ppm levels of water in phosphine using cavity ring-down spectroscopy,"* Jour. of Crys. Growth, 261, 225-230 (2004).

J. T. Hodges, *"High-resolution cavity ring-down spectroscopy of $H_2^{16}O$ at 10687.36 cm^{-1},"* ISBN 1-55752-765-2, Laser Applications to Chemical and Environmental Analysis, Annapolis, MD, February 9-11 (2004).

J. T. Hodges, H. P. Layer, W. M. Miller, and G. E. Scace, *"Frequency-stabilized single-mode cavity ring-down apparatus for high-resolution absorption spectroscopy,"* Rev. Sci. Instrum. 75, 849-863 (2004).

Temperature Measurements and Standards for Semiconductor Processing

Goals

Our goal is to enable the improved accuracy of temperature measurements in semiconductor wafer processing as prescribed in the International Technology Roadmap for Semiconductor (ITRS).

Our projeet, initiated in 1997, has resulted in improved calibration wafer technology based on thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers for in-tool radiation thermometer (RT) calibration. We have also developed improved procedures for the calibration of lightpipe radiation thermometers (LPRT) and theoretical models for the relationship between the true wafer temperature and the indicated radiance temperature.

With the completion of this work, we are now focusing on: (1) collaborating with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements, (2) developing new resistance sensors for the range 300–600 °C, and (3) understanding measurement errors when calibration wafers are used in non-isothermal or high heat-flux environments.

Customer Needs

The measurement needs of the semiconductor manufacturing industry, as stated in the ITRS, continue to evolve. Examples of recently identified challenges are:

1. The temperature dependence of present day resists limits the available critical dimension in the Post-Exposure Bake (PEB) process. Improvements will require more stringent temperature measurement and control, or improved resists (Lithography, 2005 ITRS, p. 12).

2. Fabrication of high-density, non-volatile memory is very sensitive to process temperature (Process Integration, Devices, and Structures, 2005 ITRS, p. 2).

3. Accurate process models and control algorithms require characterization of the device thermal history during a variety of processing steps (Modeling and Simulation, 2005 ITRS, p. 31)

Current needs include better temperature measurement uncertainty in post exposure bake (PEB) processing of resists, in rapid thermal processing (RTP) of wafers including silicide formation in the temperature range of 300 °C to 700 °C, and in supporting development of instrumented calibration wafers for a variety of other processing steps. Understanding differences of temperature readings between different instrumented wafers is also a high priority.

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Common Interest Group (CIG), 20 companies meeting annually since 1997. They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer.

Technical Strategy

Our research is focused on four projects that will enable the semiconductor industry to meet the roadmap requirements: (a) support our industrial collaborators in the use of test wafers with improved thin-film technology to demonstrate in-tool calibration of RTs traceable to the ITS-90, (b) develop new, accurate sensors for the 300 °C to 700 °C range, where commercial sensors are inadequate, (c) investigate effects on measurements of imperfect thermal environments with commercial instrumented-wafer technology, and (d) develop silicon-wafer emittance standards for improved temperature and emittance measurements.

Cooperative projects with Applied Materials and Atmel industries are investigating the use of the NIST calibration wafers in industrial RTP tools. These evaluations are critical for transferring the NIST developments to the semiconductor processing industry. The NIST TFTC calibration wafer has demonstrated unique capabilities in temperature measurements and in establishing traceability to the ITS-90. We have also distributed a document "Instructions for use of the NIST Thin-Film Thermocouple Calibration Wafer" in response to requests from our CIG.

DELIVERABLES: NIST TFTC calibration wafers and instructions for application of NIST calibration wafer, and joint report with Applied Materials and Atmel on LPRT calibrations. 3Q 2006

Technical Contact:
D. Ripple

"On behalf of SensArray Corporation, I express our deep gratitude to NIST for significantly contributing to advances in semiconductor lithography process optimization and control. NIST has contributed to improved CD control in lithography processes through the establishment of measurement methods and standards for wafer thermal bake cycle dynamics in resist processing. This support is just in time, as the next area of focus for photo resist processing optimization is bake cycle dynamics. Your work will be of value to every advanced semiconductor factory."

Wayne Renken, President
SensArray Corp.

Members of our CIG have also asked us to develop calibrated thin-film resistors for wafer temperature measurement from 300 °C to 600 °C. These measurements are needed for more accurate control of the silicide anneal RTP. We have undertaken the development of precision platinum thin-film resistance thermometers directly on the silicon wafers to improve the uncertainty of *in-situ* wafer temperature measurement at these temperatures. We have developed reliable methods for producing durable sensors with good performance. Work that remains is to calibrate with high accuracy the optimized sensors, to determine the best attainable hysteresis and uncertainty.

DELIVERABLES:

- Publish paper on the fabrication methods, optimization, and attainable uncertainty of thin-film Pt resistor thermometers directly on Si wafers. 3Q 2006
- Explore feasibility of using iridium films as resistance sensors up to 600 °C. 2Q 2007

As a first step in determining the sensitivity of a sensor on an instrumented wafer to a non-isothermal environment, it is necessary to measure the thermal resistance between the sensor and the silicon substrate. We have developed an apparatus in which the temporal response of a sensor to a nearly instantaneous heat pulse is measured. Simple theoretical models can be fit to the data to ascertain the thermal resistance between sensor and wafer. This simple, non-destructive technique is envisioned as a useful quality-assurance tool for manufacturers of instrumented wafers. The same techniques may be extended to study the sensitivity of various sensor designs to high, non-isotropic heat fluxes.

DELIVERABLES:

- Paper on measuring the thermal response time of commercial embedded sensors. 3Q 2006
- Conduct experiments on sensitivity of sensors in instrumented wafers to non-isotropic heat flux. 3Q 2007

Instrumented calibration wafers are now being commercially developed for temperature measurements in a variety of unusual processing environments, such as plasma processing. Modeling of the interaction of the instrumented wafer with its thermal environment is needed to meet constraints on the allowable temperature of the calibration wafers and to assist in interpretation of data obtained with the wafers.

DELIVERABLES: Assist manufacturers of instrumented wafers with heat transfer models in vicinity of sensors. 4Q 2006

Accomplishments

Development of Resistance Sensors for 300 °C to 700 °C Applications

We have explored the performance of platinum resistance thermometers deposited directly on oxide-coated silicon wafers. Our work has measured the effects of thickness and bond coat (Ti or Zr) of the Pt thin films. We have also measured the effect of ambient atmosphere (air or nitrogen) on the hysteresis and thermal coefficient of resistivity, α. The value of α was not sensitive to the annealing temperature or Ti bond-coat thickness, but did depend on the Pt thickness. Metallurgical analysis has been completed of sensors fabricated both at NIST and by commercial vendors.

Calibration of CLRTS in the Range 50 °C to 150 °C

LPRTs have been become mainstream tools for temperature measurements in the RTP community. We have calibrated LPRTs for RTP applications using a sodium heat-pipe blackbody between 700 °C and 900 °C with an uncertainty of approximately 0.3 °C (k=1) traceable to the ITS-90. Recently, cable-less LPRTs (CLRTs) offer a decisive advantage to enable radiometric measurements at lower temperatures than traditional LPRTs. The application of CLRTs can eliminate 2.0 °C or more uncertainty from the calibration scheme. We have used a Post-Exposure-Bake Test Bed at NIST to perform intercomparisons between TFTCs and the new low-temperature (50 °C to 150 °C) CLRTs. Our study has established calibration uncertainties for comparison of CLRTs against the TFTCs *in-situ*, and has established uncertainties for model-corrected CLRTs calibrated against blackbodies.

Transient Response of Temperature Sensors During the Post Exposure Bake Process

Recent studies on dynamic temperature profiling and lithographic performance modeling of the PEB process have demonstrated that the rate of heating and cooling may have an important influence on resist lithographic response. We conducted an experimental and analytical study to compare the transient response of commercial, embedded platinum resistance thermometer (PRT) sensors with surface-deposited TFTCs. A dual

instrumented wafer for PEB evaluation is shown in Fig 1. Experiments were performed on a commercial module using wafers instrumented with calibrated type-E TFTCs and commercial PRTs.

Figure 1. Wafer instrumented with PRTs and type-E thin-film thermocouples.

We measured the temperature of Si wafers in a commercial-type PEB module using both embedded PRTs and TFTCs through a typical thermal cycle from ambient, to 150 °C, and back to ambient. The transient response of the TFTCs led the PRT sensors, indicating a PRT lag (typically) of 2 °C on heating and up to 4 °C on cooling for several seconds. The wafer time constants for response were strongly affected by the air gap distance between the wafer and hot plate as expected. Thermal models were presented that showed estimates for heating time constants in good agreement with experimental data. Lithography simulation results were presented that showed the effects of transient and offset temperature profiles on CD variations.

Calibration of PRT Sensors for Instrumented Wafers

Calibration of PRTs that have been imbedded in instrumented wafers presents a challenge for the manufacturer: the wafers are much larger than commonly calibrated thermometers, the calibration process cannot contaminate wafers intended for use in a semiconductor-processing facility, and the uncertainty requirements for PEB applications are fairly demanding (standard uncertainty of approximately 0.01 °C). To validate the methods used in industry, a commercial instrumented wafer was calibrated both by NIST and by the manufacturer in the range 15 °C to 95 °C. The results were well within the stated manufacturing tolerance of the wafer and our expectations for the sensors used on the wafers.

Thermal Resistance of PRT Sensors for Instrumented Wafers

We have successfully developed a method for a relatively inexpensive measurement of the thermal resistance between resistance sensors and the underlying silicon substrate of instrumented calibration wafers. The thermal resistance is predominantly determined by the properties of the adhesives and potting compounds used to secure the sensor—a low thermal resistance is needed for the sensor to give a true reading of the substrate temperature independent of the thermal environment of the wafer. The method is non-destructive, and may be performed on used as well as new instrumented wafers to ensure that sensor attachment to the wafer substrate is acceptable for the thermal environment of use.

Recent Publications

W. A. Kimes, K. G. Kreider, D. C. Ripple, and B. K. Tsai, "*In-situ* Calibration of Lightpipe Radiometers in Rapid Thermal Processing Between 300 °C and 700 °C," in *Proceedings of the 12th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, RTP 2004, J. Gelpey, et al., eds., Portland, OR, p. 156-162, Sept. 2004.

B. K. Tsai, D. P. DeWitt, K. G. Kreider, and W. A. Kimes, "Emissivity Compensated Pyrometry for Specular Silicon Surfaces on the NIST RTP Testbed," in *Proceedings of the 12th IEEE International Conference on Advanced Thermal Processing of Semiconductors*, RTP 2004, J. Gelpey, et al., eds., Portland, OR, p. 167-172, Sept. 2004.

K. G. Kreider, D. P. DeWitt, J. B. Fowler, J. E. Proctor, W. A. Kimes, D. C. Ripple and B. K. Tsai, "Comparing the Transient Response of a Resistive-Type Sensor with a Thin-Film Thermocouple during the Post-Exposure Bake Process," *Proceedings of SPIE 29th International Symposium Microlithography*, Vol. 5378, 22-27, Santa Clara, CA, p. 81-92, Feb. 2004.

B. K. Tsai, D. P. DeWitt, E. A. Early, L. M. Hanssen, K. G. Kredier, B. J. Lee, and Z. M. Zhang, "Emissivity Standards for Improved Radiation Thermometry during Thermal Processing of Silicon Materials," *Proceedings of TEMPMEKO 2004*, Dubrovnik, Croatia, (to be published).

K. G. Kreider, D. H. Chen, D. P. DeWitt, W. A. Kimes, and B. K. Tsai, "Effects of Lightpipe Proximity on Si Wafer Temperature in Rapid Thermal Processing Tools," *Characterization and Metrology for ULSI Technology*, D. Seiler et al., eds., AIP, NY, pp. 200-204, March 2003.

K. G. Kreider, D. H. Chen, D. P. DeWitt, W. A. Kimes, and B. K. Tsai, "Lightpipe Proximity Effects on Si Wafer Temperature in Rapid Thermal Processing Tools," *Proceedings of the 11th IEEE International Conference on Advanced Thermal Processing - RTP 2003* Charleston, SC, 125-129, 2003.

B. K. Tsai, "Traceable Temperature Calibrations of Radiation Thermometers for Rapid Thermal Processing," *Proceedings of the 11th IEEE International Conference on Advanced Thermal Processing - RTP 2003* Charleston, SC, 101-106, 2003.

D. H. Chen, D. P. DeWitt, B. K. Tsai, K. G. Kreider, and W. A. Kimes, "Effects of Wafer Emissivity on Rapid Thermal Processing Temperature Measurement," *Proceedings of the 10th International Conference on Advanced Thermal Processing*, J. Gelpey, et al., eds., Vancouver, BC, pp. 59-67, 2002.

D. H. Chen, D. P DeWitt, B. K Tsai, K. G. Kreider, and W. A. Kimes, "Effects of Wafer Emissivity on Rapid Thermal Processing Temperature Measurement," *Proceedings of 8th Symposium on Temperature: Its Measurement and Control In Science and Industry*, D.C. Ripple et al., eds., AIP, NY, pp. 735-740, October 2002.

K. G. Kreider, D. P. DeWitt, D. H. Chen. W. A. Kimes, C. W. Meyer, and B. K. Tsai, "Wafer Emissivity Effects on Lightpipe Radiometry in RTP Tools," *Rapid Thermal Processing Technology Symposium* at the 201st Electrochemical Society Meeting, Philadelphia, PA, May 15, 2002, pp. 273-281.

K. G. Kreider, W. A. Kimes, C. W. Myer, D. C. Ripple, B. K. Tsai, D. C. Chen, and D. P. DeWitt, "Calibration of Radiation Thermometers in Rapid Thermal Processing Tools Using Si Wafers with Thin-film Thermocouples," *Proceedings of 8th Symposium on Temperature: Its Measurement and Control in Science and Industry*, D.C. Ripple et al., eds., AIP, NY, NY, pp. 1087-1092, October 2002.

B. K. Tsai and D. P. DeWitt, "Characterization and Calibration of Lightpipe Radiation Thermometers for use in Rapid Thermal Processing," *Proc. of 8th Symp. on Temperature: Its Measurement and Control In Science and Industry*, D.C. Ripple et al., Eds, AIP, NY, pp. 441-446, October 2002.

B. K. Tsai and D. P. DeWitt, "Improving Temperature Accuracy for Rapid Thermal Processing at NIST," *Proceedings of the NCSLI 2002 Workshop & Symposium*, 2002.

Plasma Process Metrology

Goals

Our goal is to provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the 2005 International Technology Roadmap for Semiconductors (ITRS) identifies a need for better, more predictive modeling of the impact of equipment on process results (Modeling and Simulation section, pages 15-16, and Table 122). To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, the dependence of these properties on processing equipment, and the effect of these properties on process results, further progress in model development and validation is required. The ITRS also identifies a need for development of robust sensors and process controllers (Metrology section, page 4, Table 116) which are able to convert large quantities of raw data into information useful for improving manufacturability and yield.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

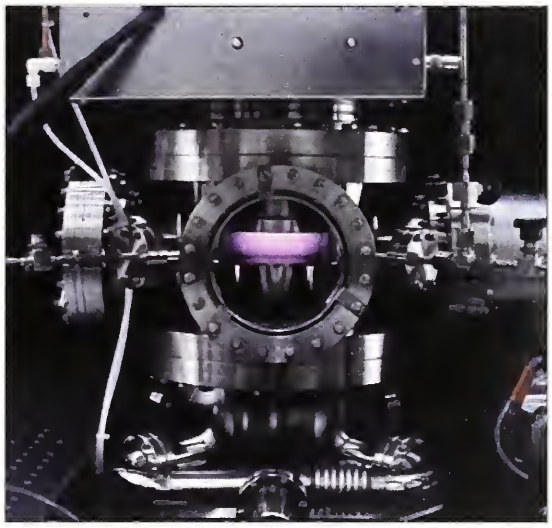

Figure 1. One of the inductive, high-density plasma reactors used in our experimental studies.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. An electrical measurement technique developed at NIST for use in process monitoring and

Technical Contacts:
M. Sobolewski
K. Steffens
E. Benck

"NIST is one of the leaders in plasma processing related research in the U.S. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek
Motorola

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries."

Bing Ji,
Air Products and Chemicals, Inc.

control applications continues to be the subject of further testing and validation. This technique relies on noninvasive, nonperturbing measurements of the radio-frequency (rf) current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of the plasma and its sheaths. To validate the technique, experiments in an rf-biased, inductively coupled plasma reactor have been performed both with and without silicon wafers loaded in the reactor. Plasma potentials, sheath voltages, total ion currents, and ion energy distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. The technique has been used to monitor long-term drift in ion energy and total ion flux. We have also monitored the more rapid changes that occur when the pressure, power, and gas flow are perturbed in ways that mimic equipment faults. Small changes in ion energy and total ion flux that occur over the course of a normal oxide etch have also been monitored. Future efforts are directed toward demonstration of the usefulness of the technique in industrial plasma reactors. In particular, such reactors are often equipped with electrostatic chucks, which may have an electrical impedance large enough to significantly affect plasma electrical characteristics. In one collaboration with an industrial company, we have characterized chuck electrical properties in a prototype commercial reactor. Additional characterization will be performed in industrial reactors and in a laboratory reactor that has been modified to have an insulating chuck similar to the electrostatic chucks used in industry. Tests will be performed in both kinds of reactors to evaluate the validity and usefulness of the NIST-developed electrical measurements, models, and analysis techniques.

DELIVERABLES: Evaluate the validity and utility of rf measurement techniques, electrical models, and analysis techniques in a laboratory reactor equipped with an insulating chuck, and in commercial plasma reactors equipped with electrostatic chucks. 3Q 2007

2. Sub-millimeter wavelength absorption spectroscopy, a sensitive and versatile diagnostic technique, will be used to study the etching process of 193 nm photoresists. The etching process of 193 nm photoresists is strongly correlated with line-edge-roughening (LER) of features produced using 193 nm photolithography. Sub-millimeter wavelength absorption spectroscopy couples to the rotational energy states of molecules and can be used to monitor a wide variety of molecular species in a plasma, including etching by-products. These measurements will be combined with the results of other research groups in order to determine methods of reducing LER in 193 nm photolithography.

DELIVERABLES: Identify and measure densities of molecules produced by plasma etching of 193 nm photoresist-coated wafers using sub-mm wavelength absorption spectroscopy. 4Q 2006

3. Dual-frequency capacitively-coupled plasma (CCP) sources are becoming increasingly important in semiconductor manufacturing processes, however, there appear to exist only limited amounts of published data on these plasma sources. Most experimental papers concentrate solely on the source etching characteristics, and numerous theory papers on dual-frequency sources show few comparisons with actual experimental data. We will address several issues related to dual-frequency sources, concentrating on how the sheath is affected by the dual frequencies. How does applying the two rf frequencies to a single electrode compare with applying the frequencies to separate electrodes? How does varying the two frequencies modify the plasma? How independent is the ion energy control and plasma production? A new diagnostic technique will be developed to help address these issues. The plasma frequency cut-off probe described below will be modified to enable it to make time-resolved electron density measurements throughout the rf cycle. Results should provide information on the nonlinear interaction of the lower frequency bias voltage with the plasma.

DELIVERABLES: Evaluate the application of the plasma frequency cut-off probe for time-resolved electron density measurements in a dual-frequency CCP source. 1Q 2007

Accomplishments

- In a collaboration with KRISS, the Korea Research Institute of Standards and Science, a new method for measuring electron number density in plasmas, the wave cut-off method, has recently been implemented in NIST laboratories. Unlike Langmuir probe measurements, which are commonly used for measuring electron density, cut-off measurements do not suffer from problems with

rf compensation or deposition of insulator layers. Comparisons performed in one of our inductively coupled plasma reactors showed good agreement between electron densities measured by the cut-off probe and by a Langmuir probe. The accuracy of the cut-off probe, based on theoretical arguments, is believed to be greater than the Langmuir probe. The cut-off probe has been used to characterize the spatial variation of the electron density in the inductively coupled reactor and the effect of rf substrate bias on the electron density. Interest in the bias effect has been stimulated by recently proposed, new methods for rf biasing, such as double-frequency bias and nonsinusoidal bias, which may contain Fourier components at frequencies higher than those previously used for biasing. Our measurements showed that even at bias frequencies as high as 30 MHz, the effect of bias on electron density is small, and therefore that nearly independent control of ion energy and ion flux can be maintained even at such high frequencies. Simple analytic models that describe the effect of bias on electron density, which would be useful for estimating such effects under other experimental conditions in other plasma reactors, have been derived and validated by the cut-off measurements.

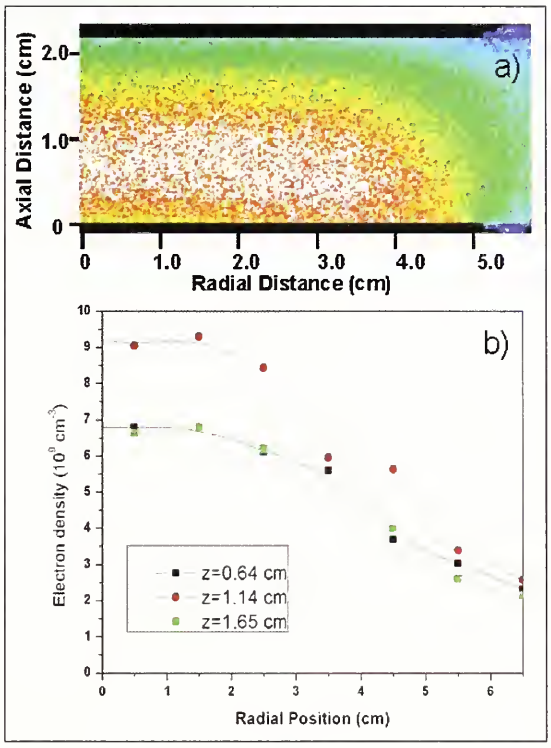

Figure 2. Measurements taken in 100 mTorr, Ar/CF_4 plasmas of a) CF density by PLIF and b) plasma density radial profiles by the cut-off probe technique.

■ In addition, we have combined the cut-off probe electron density measurements with two-dimensional (2-D) optical measurements in capacitively-coupled Ar/CF_4 plasmas (Fig. 2). Planar laser-induced fluorescence (PLIF) was used to measure 2-D density maps of the reactive radical CF. The 2-D images of spontaneous plasma emission from excited species within the plasma were also measured. Radial and axial profiles of electron density, CF density, and plasma emission were measured in CF_4/Ar plasmas and compared to determine the nature of the correlation of reactive species spatial distributions with electron density distributions.

■ Spatially and temporally resolved measurements of optical emission from a dual-frequency capacitively-coupled plasma source have been made. Although these types of sources are becoming increasingly important in semiconductor manufacturing processes, there appears to be only a limited amount of published data related to them. This investigation utilized an imaging spectrometer coupled to an intensified CCD camera to image the vertical distribution of the optical emission from a single atomic transition as a function of time, synchronized with the lower frequency rf bias voltage. This provides insight into the non-linear coupling of the rf bias to the plasma production. It was found that electronegative feed gases (such as CF_4) significantly alter the temporal behavior of the plasma emission, indicating a change in the electron heating or plasma production processes caused by the rf bias voltage. The temporal behavior of the optical emission was dependent on gas pressure. These results are being correlated with the voltage and current waveforms at the electrode surfaces which are simultaneously recorded.

Many industrial plasma etchers are equipped with optical emission spectrometers, which have proven useful for endpoint detection, fault detection and classification, and automatic process control. We have performed experiments in which optical emission measurements are combined with noninvasive current and voltage measurements. Optical emission complements the electrical measurements by providing information about drift or other changes in the chemical species within the plasma—information that would be difficult or impossible to obtain solely from electrical measurements. We have made a series of measurements in CF_4/Ar plasmas to investigate the correlation between electrical and optical emission changes in the plasma which occur as a function of time during an oxide etch and during chamber conditioning. We measured emission from Ar, F, CF, CF_2 and SiF. Changes are observed in the optical emission from many species and in electrical parameters as the etch endpoint is reached (Fig. 3). A particularly strong correlation was found between the plasma impedance and F emission.

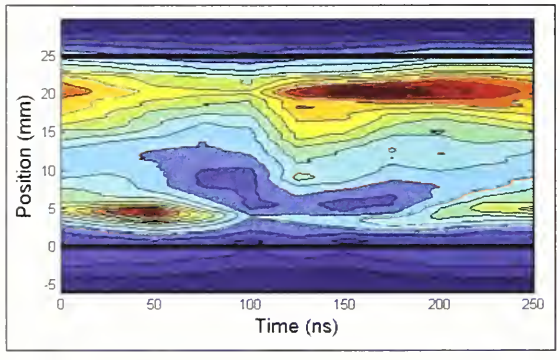

Figure 3. Time-resolved vertical distribution of optical emission (750nm) from a dual-frequency capacitively-coupled plasma. The plasma was created using 26 W at 13.56 MHz applied to the upper electrode and 9 W at 2 MHz applied to the lower electrode. A gas mixture of CF_4:Ar:O_2 was used with a ratio of 2.0:7.5:0.5. The solid horizontal lines indicate the edges of the electrodes.

■ The NIST-developed, noninvasive, model-based electrical technique for monitoring ion energy and total ion flux has recently been validated in actual etching conditions in CF_4/Ar plasmas (Fig. 4). Unlike previous validations, performed with no wafer present, the recent validations were performed with silicon wafers — oxidized and bare — loaded into the reactor. The wafer, as well as the contact between the wafer and the electrode on which it rests, both contribute an electrical

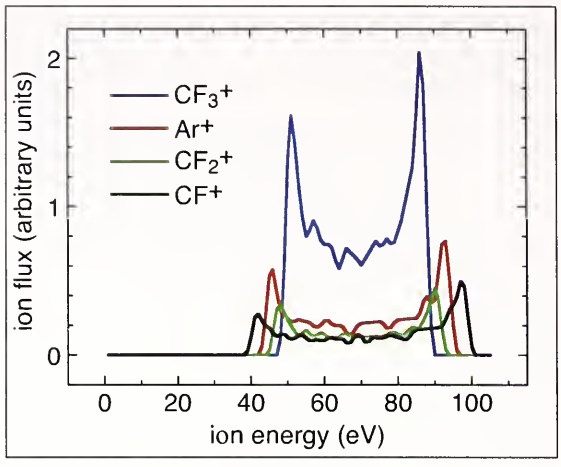

Figure 4. Ion energy distributions from noninvasive electrical measurements, determined in real-time during an oxide etch in an Ar/CF_4 plasma.

impedance which, if unaccounted for in the model, can cause errors in the ion energy distributions and total ion flux obtained from the noninvasive technique. At low rf bias frequencies < 100 kHz, the contributed impedance was large, resulting in substantial errors in the noninvasive results. Nevertheless, at bias frequencies of 1 MHz or higher, which are more typical of semiconductor manufacturing, the wafer and wafer contact contribute only a few ohms of impedance, resulting in an uncertainty in noninvasive ion energies of only a few electron volts. The speed of the analysis algorithms has also recently been greatly increased, making it possible to monitor changes in ion energy and total ion flux with a time resolution on the order of 1 second. In recent demonstrations, the speeded-up technique has been used to monitor small changes in ion energy and total ion flux that occur over the course of a "normal" oxide etch, as well as larger changes that occur when the pressure, power, and gas flow were perturbed in ways that simulate equipment faults.

■ Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST "Electron Interactions with Plasma Processing Gases" database. This Web site has experienced tens of thousands of hits throughout its history.

Recent Publications

M. A. Sobolewski, *"Noninvasive monitoring of ion energy drift in an inductively coupled plasma reactor,"* J. Appl. Phys. 97, article #033301, 1-12 (2005).

K. L. Steffens and M. A. Sobolewski, *"2-D imaging of temperature in CF_4 plasmas,"* IEEE Transactions on Plasma Science, 33, 370-371 (2005).

K. L. Steffens, M. A. Sobolewski, *"2-D Temperature Mapping in Fluorocarbon Plasmas,"* AIP Conference Proceedings, Vol. 788: Characterization and Metrology for ULSI Technology, (American Institute of Physics, Melville, NY, 2005) pp. 333-337.

M. A. Sobolewski, *"Noninvasive monitoring of ion energy in an inductively coupled plasma reactor,"* AIP Conference Proceedings, Vol. 788: Characterization and Metrology for ULSI Technology, (American Institute of Physics, Melville, NY, 2005) pp. 319-323.

M. A. Sobolewski, *"Monitoring sheath voltages and ion energies in high-density plasmas using noninvasive radio-frequency current and voltage measurements,"* J. Appl. Phys. **95**, 4593-4604 (2004).

K. L. Steffens and M. A. Sobolewski, *"A technique for temperature mapping in fluorocarbon plasmas using planar laser-induced fluorescence of CF,"* J. Appl. Phys. **96**, 71-81 (2004).

M. Edamura and E. C. Benck, *"Effects of voltage distribution along an induction coil and discharge frequency in inductively coupled plasmas,"* J. Vac. Sci. Technol. A **22**, 293-301 (2004).

Assessment of Measurements and Standards for Gas Phase Processes in Semiconductor Device Manufacturing

Technical Contact:
R. Berg

Goals

New materials used in gas phase processes will require new measurements and standards for the efficient delivery of those materials to the wafer surface. The National Institute of Standards and Technology (NIST) will supplement its ongoing project to measure the thermophysical properties of semiconductor gases with a new effort to measure the relevant properties of liquid precursors. NIST will identify the properties of greatest interest, identify existing accurate data for those properties, and devise techniques to measure those properties where accurate data do not exist. The data will improve the modeling of chemical vapor deposition, the calibration of mass flow controllers, and the design and use of bubblers and other devices that deliver precursor vapors. This project will be coordinated with continued work on standards for gas flow at rates less than 1000 μmol/s (about 1 standard liter per minute).

Customer Needs

Precursors for chemical vapor deposition are frequently liquid compounds that, until recently, were either rare or nonexistent. Their vapors are delivered to the process chamber either by direct injection (flash evaporation) or by bubbling a carrier gas through the liquid held in a "bubbler". Accounts from companies that either sell liquid precursors or sell the associated process equipment suggested an industrial need for improved property data of these specialty chemicals. Designers and users of mass flow controllers, bubblers, and other gas and liquid delivery devices could use such data to optimize device performance. An ongoing project at NIST has produced accurate property data for semiconductor process gases such as boron trichloride and nitrogen trifluoride. The project, which received guidance from a NIST-organized workshop in 2000, has posted data for specific heat, second virial coefficient, viscosity, and other properties at *properties.nist.gov/fluidsci/semiprop/*. The new effort will include liquid precursors, with likely measurements being vapor pressure and liquid viscosity.

Vapor pressure is the most important physical property of liquid precursors. It determines the concentration of the precursor-carrier mixture produced by a bubbler, and it sets a lower limit on the wall temperature of the delivery line and process chamber. Although high vapor pressures are preferred, the acceptable range is wide. For example, when heated to 100 °C, the vapor pressure of the widely used liquid TEOS (tetraethyl orthosilicate) is PV(100 °C) = 12 kPa. In contrast, a candidate precursor might be considered even if its vapor pressure were 100 times lower, namely even if PV(100 °C) = 0.1 kPa.

Other important properties include liquid viscosity and thermal stability. Viscosity can affect the performance of injection systems. Thermal stability is important because the precursor's decomposition rate may limit the process's upper operating temperature and thereby the vapor pressure.

Technical Strategy

NIST will identify the gaps between property needs and available data and then begin filling those gaps with new measurements and data compilation. Desired results include new or enhanced NIST databases, new NIST capabilities to measure the vapor pressure and liquid viscosity of liquid precursors, and the transfer of those capabilities to industry.

DELIVERABLES: Identify the most important physical properties of liquid precursors. 2Q 2006

The most important physical properties are vapor pressure, liquid viscosity, and thermal stability, followed by others, density and such as heat of vaporization. Ancillary concerns include materials compatibility and suspended particles.

DELIVERABLES: Identify existing property data and assess its quality. 2Q 2006

Existing data can be found in technical literature, the NIST Chemistry WebBook, NIST standard reference database 87, and other databases. The applicability of estimation techniques, such as group contribution methods, also will be examined.

DELIVERABLES: Organize and lead workshop at Semicon West to identify the gaps between the needed data and the available data for physical properties such as vapor pressure, viscosity, and specific heat. 3Q 2006

Workshop discussion topics:

(1) Which gases should be measured next?

(2) Which liquid precursors should be measured?

(3) What properties of liquid precursors are most important?

(4) Are the data efficiently available?

DELIVERABLES: Identify suitable methods to measure vapor pressure and decomposition. Procure and assemble apparatus. 4Q 2006

Avoiding mercury and other incompatible materials eliminates many classic techniques.

Accomplishments

We continue to broaden the uses of the standards for gas flow that were developed recently at NIST. The model for the quartz capillary flow meter was applied to a ratio viscometer that yielded values of unprecedented accuracy (0.084 %) for the viscosity of argon at temperatures from 200 K to 400 K. Similar results are expected for hydrogen, methane, ethane, and xenon. A similar flow meter will be used to provide a reference gas flow for calibrating spinning rotor pressure gauges at moderate vacuum.

Recent Publications

E. F. May, M. R. Moldover, R. F. Berg, and J. J. Hurly, "Transport properties of argon at zero density from viscosity-ratio measurements," *Metrologia* 43, 247-258 (2006).

Analysis Tools and Techniques Program

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip approaches 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements. Those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed, but measurements cannot be done is critical. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed.

Thin-Film X-Ray Metrology for Microelectronics

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Goals

This multi-year collaborative effort between SEMATECH and NIST will provide the semiconductor community with the measurement methodology and calibration capability for accurate thin film characterization using X-Ray Reflectometry (XRR).

Customer Needs

In recent years, the semiconductor industry has driven scientific advancement towards processing nanometer-scale material coatings with unprecedented uniformity in thickness, composition control, and unique electrical and mechanical properties. Nanotechnology represents the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as High-Resolution X-Ray Diffraction (HRXRD) and XRR that permit the quantitative profiling of thin film characteristics, such as thickness, density profile, composition, roughness, and strain fields. With the XRR method in particular, parameter modeling by conventional methods can be an intractable problem, involving deconvolution of instrument response, data model theory, model selection, and model refinement/fitting, which has prevented the realization of the technique's potential in the characterization of nano-dimensional thin film structures. This effort addresses the mounting industry call for accuracy in thin film characterization (in particular; thickness, density, and roughness determination).

Technical Strategy

This fundamental XRR effort involves two parallel characterization projects being performed on identical, temporally stable, multilayer artifacts supplied by SEMATECH. The NIST project consists of in-house XRR and HRXRD characterization with Système International (SI) traceable measurement instrumentation and SI traceable, first principles data modeling including Bayesian analysis providing refinement of instrumental and model parameters as well as structural model selection. In parallel to this NIST measurement project, SEMATECH will measure or have measurements performed using commercial "in-line" XRR instrumentation and NIST will analyze these data using commercial software to address limitations to commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimations for a given XRR structural analysis approach and instrumentation. This work will take approximately three years to address the issues discussed [FYs 05, 06, and 07]. The progress in FY05 included a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation. FY06 deliverables will explore the application of an approximate Bayesian model selection method to compare the relative probability of different structural models for measured XRR data. Preliminary results with simulated XRR data have shown success in determining the initial structural model used to generate the simulated data.

NIST XRR Study – The NIST 'standard' approach for improving accuracy and precision in a measurement technique involves the generation of a Standard Reference Material (SRM). Figure 1 shows the three parallel research aspects needed for the development of an XRR SRM: (1) the

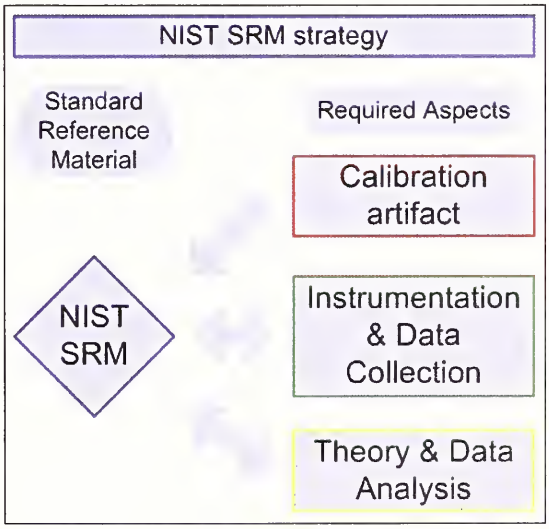

Figure 1. Aspects necessary for a NIST Standard Reference Material. All aspects are essential to provide structural parameter SI traceability.

manufacture of a robust thin film calibration artifact with a high degree of temporal stability and contamination and/or oxidation resistance, (2) the development of SI traceable measurement instrumentation, (3) the creation of an SI traceable, first principles data analysis approach. Figure 2 shows the current status of steps required to address these aspects for our XRR SRM project.

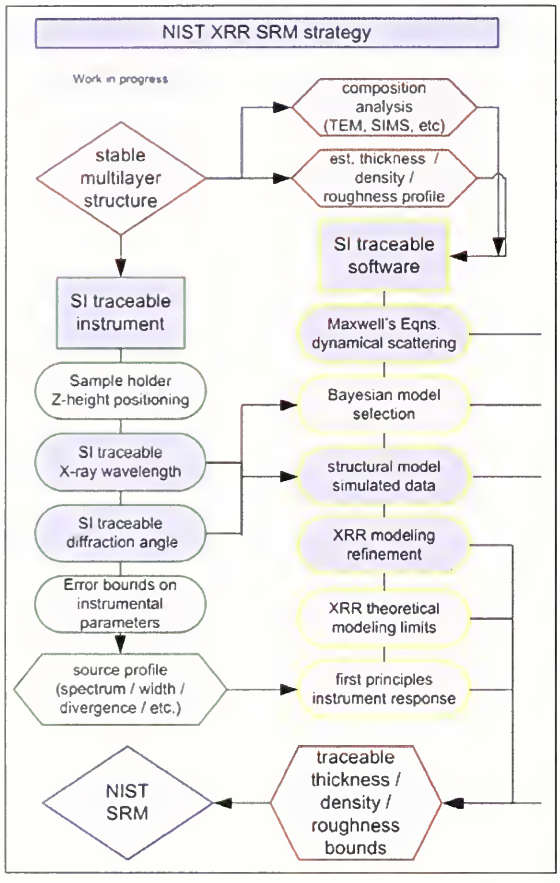
NIST XRR SRM strategy
Work in progress
composition analysis (TEM, SIMS, etc)
stable multilayer structure
est. thickness / density / roughness profile
SI traceable software
SI traceable instrument
Maxwell's Eqns. dynamical scattering
Sample holder Z-height positioning
Bayesian model selection
SI traceable X-ray wavelength
structural model simulated data
SI traceable diffraction angle
XRR modeling refinement
Error bounds on instrumental parameters
XRR theoretical modeling limits
source profile (spectrum / width / divergence / etc.)
first principles instrument response
NIST SRM
traceable thickness / density / roughness bounds

Figure 2. NIST XRR SRM strategy. This flowchart illustrates the key steps in the NIST XRR SRM development project. The light areas indicate work in progress. The outline colors indicate the appropriate aspect of the SRM development process for each step.

This collaborative effort with SEMATECH allows us to examine semiconductor industry relevant structures as potential candidates for an XRR calibration artifact. NIST has also engaged other National Metrology Laboratories in an effort to assess the temporal stability of international NML pre-standards. Both PTB of Germany and NMIJ/AIST of Japan have provided us with structures for comparative XRR analysis. This cooperative study will help gauge which thin films structures provide stable, well defined, refinement parameters suitable for SI traceable modeling.

NIST has applied considerable resources into the development of SI traceable X-Ray Reflectometry instrumentation. Over the past seven years, NIST/MSEL has constructed the Ceramics Division Parallel Beam Diffractometer (CDPBD) for SI traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (see Fig. 3). Over a similar timeframe, the Physics Laboratory developed the Physics Laboratory X-Ray Reflectometer (PLXRR) specifically for XRR characterization of semiconductor thin-film artifacts. As of FY06, we will be working in cooperation with the Physics Laboratory, to integrate the PLXRR into the XRR SRM effort allowing us cross-laboratory measurement comparison in our certification process.

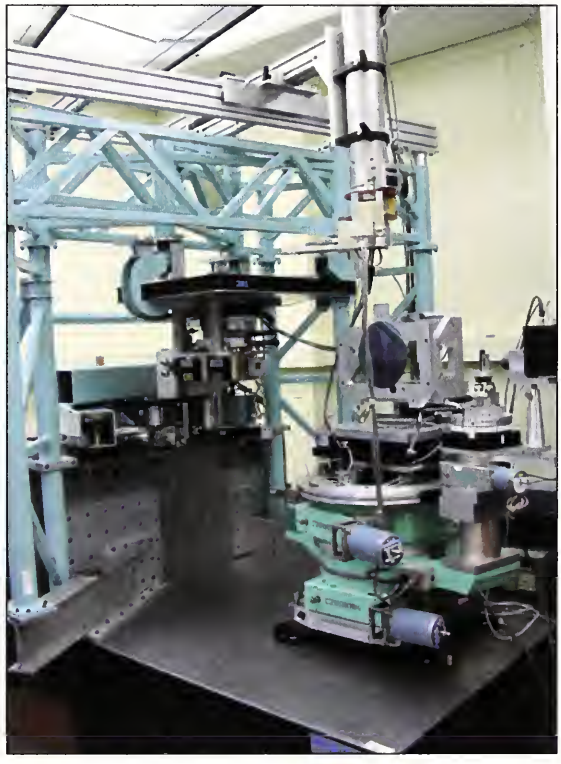

Figure 3. Ceramics Division Parallel Beam Diffractometer (CDPBD). Showing a rotating anode X-ray source (center left), monochromator for generating parallel/monochromatic X-rays (upper center), angle-encoded rotation stages for measuring diffraction angles (lower right) and receiving optics/detector (center right). In order to achieve accuracy in angle measurements and X-ray wavelength stability, numerous design features of varying complexity are present ranging from a "floating" platform holding the X-ray source to a hanging second rotation stage (top center) designed specifically to rotate the cables for the diffraction rotation stages.

SI traceability in either lattice parameter (XRD) or film thickness (XRR), d, requires simultaneous traceability in X-ray wavelength, λ, and diffraction angle, θ, following Bragg's law of diffraction: $2d = n\lambda / \sin(\theta)$. The present NIST instrument development project involves addressing SI traceability aspects for both the diffraction angle and wavelength measurement on the CDPBD. Establishing SI traceability of the diffraction angle requires implementing optical encoding on the two rotation stages used to move the sample and detector. The optical encoder errors are then "mapped" using an external angle reference to generate SI traceability error bounds for each axis. The rotation stages presently have accuracy bounds of $\pm$ 2.0 µrads ($\pm$ 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers is currently underway to achieve an approximate one order of magnitude improvement in accuracy by next year (FY07). Determining SI traceability in wavelength involves constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction. The CDPBD uses a monochromator with Si (220), 2/4-bounce channel-cut crystals to filter the direct source into a source of highly parallel, single energy X-rays. SI traceability in X-ray wavelength from our source will be performed using an SI traceable reference crystal (with measured relative standard uncertainty of 3 in 10^{-8}). The X-ray wavelength for our instrumentation currently has a relative standard uncertainty of $\approx$1 in 10^{-5} (FY06). The accuracy error bounds and instrument parameters from the wavelength and angle determination studies will provide an overall instrument response function which will be incorporated into NIST XRR profile modeling. The same instrumental parameters will establish guidelines for response profile modeling of commercial instrumentation (FY07 deliverable).

NIST is currently developing first principles, SI traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is essentially an "inverse problem" wherein we select input parameters for a "guessed" structural model. This model is then used to simulate data that is compared with measured data and "Goodness of Fit" parameters are determined. This process is repeated until a "best fit" or best "Goodness of Fit" is found and the "best fit" model parameters become the "refined" model parameters used to describe the real structure. Three major questions limit the effectiveness of this current XRR modeling approach: (1) How do we accurately simulate the data using a structural model? (2) How do we know which structural model describes the measured structure? (3) How do we accurately compare simulated and measured data? The NIST software development effort will attempt to answer each of these questions.

To address the model data simulation issue, we have developed XRR theory from Maxwell's equations explaining all approximations and constraints required for the XRR modeling method. This approach will in the future combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in derived refined parameters (FY07+). To address the question of model accuracy, we are implementing a Bayesian/Maximum Entropy analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural assumptions in any XRR analysis (approximate method in FY06). Addressing the third question is of considerable interest with current commercial refinement approaches which often use dissimilar "chi squared" or model/simulation minimization criterion for overall refinement "figures of merit" such that comparison between refinement software packages is impossible. NIST will perform a rigorous analysis of current refinement approaches (such as genetic algorithms which are popular in commercial software for their speed advantage, Monte Carlo Markov Chain, simulated annealing, etc.) and of applicable minimization criterion to develop a consistent refinement approach for NIST modeling (FY07).

NIST/SEMATECH XRR Study – The NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis.

The NIST/SEMATECH project combines measurements with commercial "in-line" XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration work with SEMATECH allows interface and

calibration transfer between NIST SI traceable measurements and "in-line" instrumentation. NIST will then use results from NIST SI traceable measurements, SEMATECH commercial measurements and modeling, and NIST SI traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or provide detailed instrument response functions directly. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument "corrections" to the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring (FY07+ deliverable).

Project Deliverables – The final project results available to SEMATECH will include XRR error budget estimations based on NIST XRR software and the calibration artifacts necessary for optimizing the performance of commercial "in-line" and laboratory XRR instruments. Accuracy and precision estimations provided by NIST software will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation. Calibration artifacts measured on NIST SI traceable instrumentation will allow routine system monitoring, alignment calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional XRR characterization of multilayer structures which exhibit well-established composition and uniformity (FY07+ deliverables).

Our deliverables schedule for the calendar year 3/2006-3/2007 time frame follow:

DELIVERABLES:

- NIST analysis of SEMATECH measurement. 2Q 2006
- Approximate Bayesian model selection method. 2Q 2006
- NIST analysis of SEMATECH measurements. 4Q 2006
- Approximate Bayesian interface selection method. 2Q 2006

Accomplishments

■ Last year, the CDPBD moved to equipment space in the Advanced Measurements Laboratory (AML at NIST) which provides instrument temperature stability of ± 0.02 °C. Preliminary calibration of the angle measurement has been assessed for uncertainty determination in data modeling (current accuracy determination has been completed) and improvements using a new compensation approach (being developed through a joint National Metrology Laboratory effort with PTB) will be implemented in the future (FY07). First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software was completed (FY06) and a dynamical scattering based model has been implemented with Monte Carlo Markov Chain (MCMC) methods for structural parameter refinement and formal parameter uncertainty analysis (2Q 2006). A second round of measurements on SEMATECH artifacts measured by both conventional and NIST traceable XRR systems will be completed this year (2Q 2006).

■ *FY06 Technical transfer: Approximate Bayesian approach to model selection* – Preliminary studies into the use of an approximate Bayesian approach for assigning relative probabilities between two structural models was completed last spring (FY05). This study was done with simulated XRR data sets. In FY06, this data analysis approach is being expanded to apply to data with included instrumental parameters. Initial results with this method stirred considerable interest due to its ease of implementation with conventional XRR packages. A requested deliverable in FY06 is the recipe for this approach on both structural

model selection and interface type selection. In Fig. 4a, we show simulated XRR data from a two-layer structural model with included Poisson statistical noise. Two different structural models were used in data refinement: a single-layer model (Fig. 4b) and a two-layer model (Fig. 4c). As expected, the two-layer model (Fig. 4c) showed to be most probable for each statistical noise level. The impressive feature in the study was that the probability ratio between the two models favored the two-layer case by many orders of magnitude for each level of statistical noise. This approximate method cannot give the absolute probability of a model. It can only provide a comparison of probabilities between two models, which is often a crucial piece of information (*i.e.*, is there an interface or surface oxide present?). This recipe will be available to SEMATECH later this summer (2Q 2006).

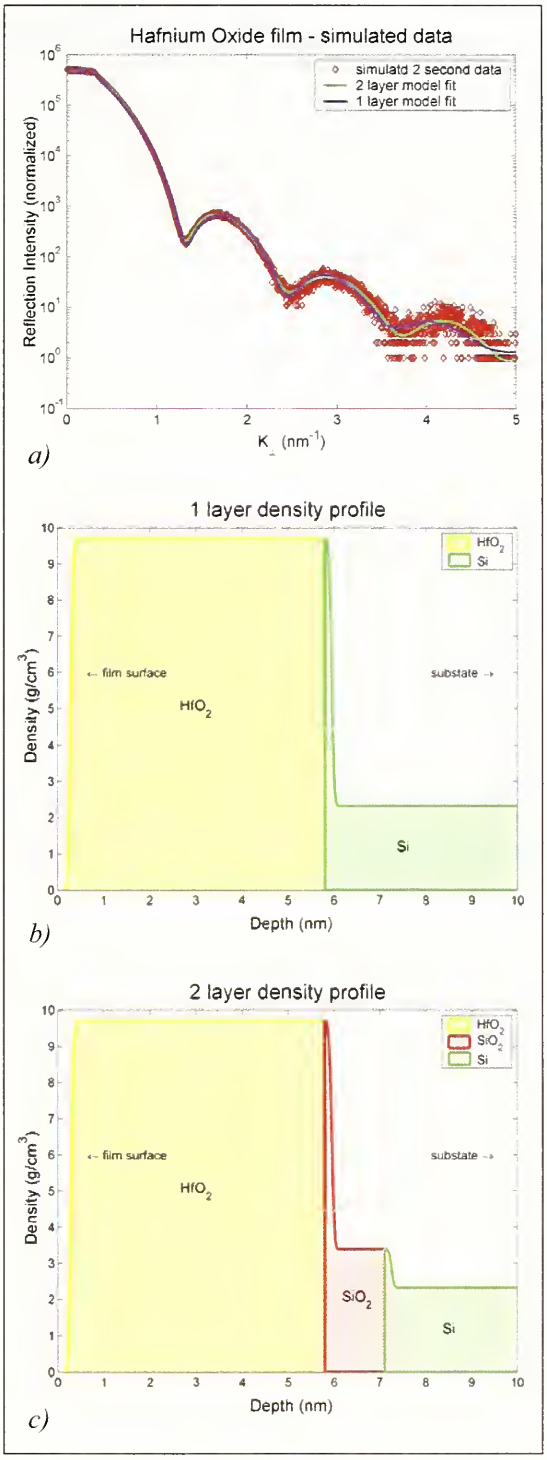

Figure 4. Example of the Bayesian Model selection method. The probability of different structural models can be compared to find the most probable structure for given data. In this example, a two-layer structural model was used to simulate X-Ray Reflectometry data (4a). A single-layer model (4b) and a two-layer model (4c) were used for data characterization and a Bayesian Model selection comparison approach was attempted. The two-layer model was shown to be the "correct" model for all two-layer simulated data at typical measurement statistical noise levels.

Collaborations

SEMATECH – P.Y. Hung & Alain Diebold

PTB, Precision Metrology – Peter Thomsen-Schmidt

Bede Scientific Inc. – Keith Bowen & Matthew Wormington

Bruker AXS – Arnt Kern & Alan Coelho

Jordan Valley Semiconductors – Dileep Agnihotri

NMIJ/AIST – Toshiyuki Fujimoto

Rigaku MSC – Tom McNulty & Joe Formica

Technos International – Henry Yeung

Recent Publications and Presentations

N. Armstrong, D. Windover, A. Henins, J. P. Cline, *"NIST X-Ray Metrology and SRM 1979 for naoncrystallite size broadening"* – invited presentation at CSIRO, Sydney, Australia (November 2005).

D. Windover, N. Armstrong, J. P. Cline, *"Prototype Standards for X-Ray Reflectometry: an international perspective"* – invited colloquia at PTB, Braunschweig, Germany (September 2005).

D. Windover, N. Armstrong, J. P. Cline, *"Prototype Standards for X-Ray Reflectometry: an international perspective"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2005).

N. Armstrong, J. P. Cline, J. Ritter, and J. Bonevich, *"SRM 1979: The NIST SRM for nanocrystallite size broadening"* – invited presentation at Denver X-Ray Conference, Denver, CO (August 2005).

D. Windover, N. Armstrong, J. P. Cline, P. Y. Hung, and A. Diebold, *"Characterization of Atomic Layer Deposition using X-Ray Reflectometry"* – poster/paper at 2005 International Conference on Characterization and Metrology for ULSI Technology, Dallas, TX (March 2005).

N. Armstrong, W. Kalceff, J. P. Cline, and J. Bonevich, *"A Bayesian/Maximum Entropy method for certification of a nanocrystallite-size NIST Standard Reference Material"* – Ch. 8 in Diffraction analysis of the microstructure of materials, pp. 187-227, Ed. P. Scardi and E.J. Mittemeijer, Springer-Verlag, Berlin, ISBN: 3-540-40519-4 (2004).

N. Armstrong and P. Lynch, *"Determining the dislocation contrast factor for X-ray line profile analysis"* – Ch. 10 in Diffraction analysis of the microstructure of materials, pp. 249-307, Ed. P. Scardi and E.J. Mittemeijer, Springer-Verlag, Berlin, ISBN: 3-540-40519-4 (2004).

N. Armstrong, W. Kalceff, J. P. Cline, J. Bonevich, *"Bayesian inference of nanoparticle-broadened X-ray line profiles"* – J. NIST Research, 108(5), pg 155-178 (2004).

N. Armstrong, M. Leoni, M. Scardi, *"Some concerns regarding the Wilkens' model for dislocation line broadening"* – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic, (September 2004).

N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, *"Status of the NIST Nanocrystalline Size SRM–1979"* – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic (September 2004).

N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, *"Bayesian characterization of nanoparticles from line profile"* – presentation at Denver X-Ray Conference, Denver, CO (August 2004).

N. Armstrong, W. Kalceff, J. P. Cline, J. Bonevich, P. A. Lynch, C. C. Tang, S. A. Thompson, *"X-ray diffraction characterization of nanoparticle size and shape distributions: – Application to bimodal distributions"* – Proceedings of the 28th Annual Condensed Matter & Material Meeting, Wagga, Australia (February 2004).

Electron Microscope Tomography of Electronic Materials

Technical Contacts:
Z. H. Levine
J. H. Scott

Goals

Enable the use of three-dimensional imaging for thick samples using commercial scanning transmission electron microscopes (STEM). Typical samples include porous low-κ dielectrics, two-layer interconnect samples, and photonic band gap materials.

Customer Needs

The NTRS/ITRS has recognized the need for three-dimensional imaging of interconnects for several years. In this study, our principle objective is to determine the morphology of pores in low-κ dielectric material. Two aspects of the pore distribution are critical: (a) the largest pores may lead to failure of the dielectric (*e.g.*, short circuits), and (b) the connectivity of the pores is important to understand the transport of chemicals during the fabrication of the interconnect.

The potential solutions and major challenges for interconnect are discussed in the 2005 International Technology Roadmap for Semiconductors Update on pages 6 and 7 of the Interconnect Section. Three dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.

Technical Strategy

1. We have various theoretical capabilities in hand, including the ability to perform 3D Monte Carlo simulations, the ability to perform tomographic reconstructions using an in-house 3D Bayesian code for tomographic reconstruction which permits an arbitrary transmission-thickness relation. Other capabilities are under development including a tomographic alignment program. An example is shown in Fig. 1.

DELIVERABLES: Tomographic alignment program which will report the tilt axis direction on the unit sphere. 2Q 2006

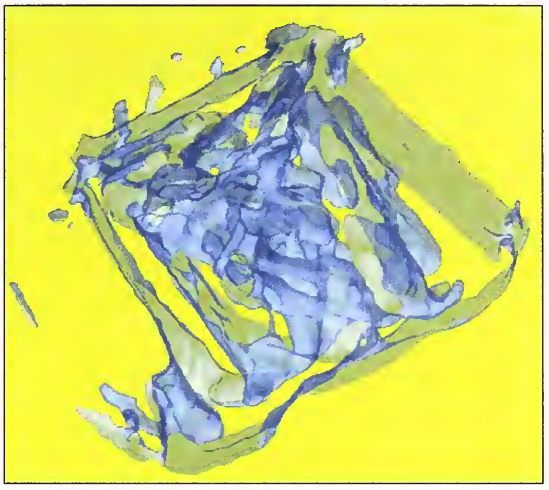

Figure 1. Tomographic reconstruction of a photonic band gap sample. An interconnecting network of material and void is present in the center of the figure. The bands on the outside are from the platinum overlayer added to protect the sample during preparation by a focused ion beam.

2. In parallel, we will develop theoretical expertise for the effects of coherence on the samples, including understanding when Bragg diffraction is significant for tomography, and to develop simulations of coherent beam illumination, and strategies for beam rocking to reduce said coherence while preserving a sufficiently straight beam for standard tomographic algorithms.

Accomplishments

- Principle accomplishments include: creation of 3D Bayesian code for tomographic reconstruction; completion of prototype code for identification of rotation axis on the unit sphere and alignment for tomography; further development of 3-D Java Monte Carlo simulation of these complex geometries, allowing understanding of how observed X-ray intensities into composition, shown in Fig. 2 (page 150).

Collaborations

International Sematech, Brendan Foran, preparation of low-κ samples, electron microscopy.

Chris Soles and Hae-Jeong Lee, NIST, MSEL, Polymers Division; low-κ samples

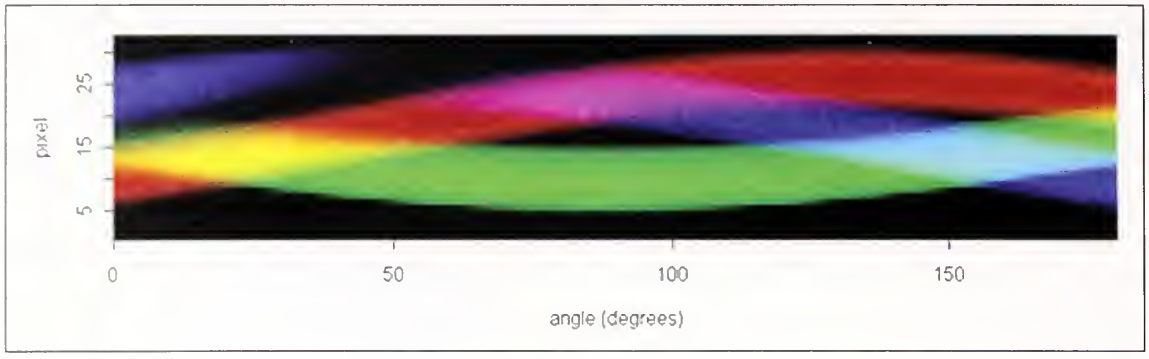

Figure 2. 3-D Java Monte Carlo simulation of interconnect phantoms and observed X-ray emission (Cu=red Al=blue SiO_2=green) from 0 degree to 180 degree tilt.

Accurel, Inc. Preparation of focused ion beam sections from low-κ samples

Lucent Technologies, Shu Yang; preparation of photonic band gap material.

Recent Publications

Z. H. Levine, *"An X-Ray Tomography Primer,"* Electronic Device Failure Analysis 7, 26 (2005).

Z. H. Levine, *"Theory of Bright-Field Scanning Transmission Electron Microscopy,"* J. Appl. Phys. 97, 033101 (2005).

Z. H. Levine, S. Grantham, D. J. Patterson, I. McNulty, I. C. Noyan, and T. M. Levin, *"Imaging material components of an integrated circuit interconnect,"* J. Appl. Phys. 95, 405 (2004).

Z. H. Levine, *"Tomography in the Multiple Scattering Regime of the Scanning Transmission Electron Microscope,"* Appl. Phys. Lett. 82, 3943 (2003).

Z. H. Levine, J. A. Gao, S. Neogi, T. M. Levin, J. H. Scott, and S. Grantham, *"Parallax measurements of an integrated circuit interconnect using a scanning transmission electron microscope,"* J. Appl. Phys. 93, 2193 (2003).

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

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L. R. Vale

Goals

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator. We are presently simplifying this refrigerator to reduce system costs and increase the accessibility of microcalorimeter technology.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Promising new technology such as high-energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMS located in the clean room." **2003 International Technology Roadmap for Semiconductors**

Technical Strategy

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now

been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters for increased collection area and count rate have been demonstrated and their energy resolution is comparable to single sensors. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with other partners in disseminating the technology.

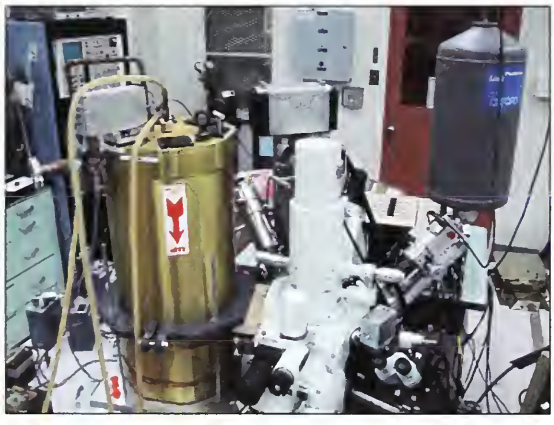

Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Prepare for the eventual transfer to CSTL of an array microcalorimeter system. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry. 4Q 2006

2. The adiabatic demagnetization refrigerator that provides 0.1 K operating temperatures is a crucial part of a microcalorimeter system. To date, adiabatic demagnetization refrigerators have been precooled to 4 Kelvin with liquid nitrogen and helium. However, the use of liquid cryogens is an obstacle to potential microcalorimeter users. Consequently, it is desirable to precool the adiabatic demagnetization refrigerator with a push-button mechanical cryocooler whose only consumable is electricity.

DELIVERABLES: Design and build an adiabatic demagnetization refrigerator cooled by a pulse tube mechanical cryocooler. Understand and minimize the electrical and mechanical effects of the cryocooler on microcalorimeter operation. 1Q 2006

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive ^{3}He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES: Demonstrate the cooling of an electrically-separate piece of thin-film electronics using a tunnel-junction refrigerator that could be coupled to a simple ^{3}He refrigerator. 2Q 2006

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated and been used to successfully read out eight microcalorimeters under X-ray illumination. Significant increases in multiplexer bandwidth and pixel-handling capacity are possible based on evolutionary design improvements.

DELIVERABLES: Demonstrate improved SQUID multiplexer and multiplexed operation of larger numbers of microcalorimeters under X-ray illumination. Characterize multiplexer performance and design next-generation system. 4Q 2006

Accomplishments

- We designed and built an adiabatic demagnetization refrigerator that is precooled by a mechanical cryocooler. This simple and compact system is operated by the push of a button and requires no liquid cryogens. Because the cryocooler achieves a base temperature of 2.8 Kelvin, lower than that of liquid helium, the operating time of the demagnetization refrigerator below 0.1 K is significantly extended. In addition, we have demonstrated undegraded operation of a high resolution microcalorimeter in the electromagnetic

environment of the cryocooler and its control electronics. We have also begun to characterize the effects of the mechanical vibration of the crycooler on other instruments such as a scanning electron microscope. A photograph of the pulse tube cooled – demagnetization refrigerator undergoing vibration testing on an electron microscope is shown in Fig. 2.

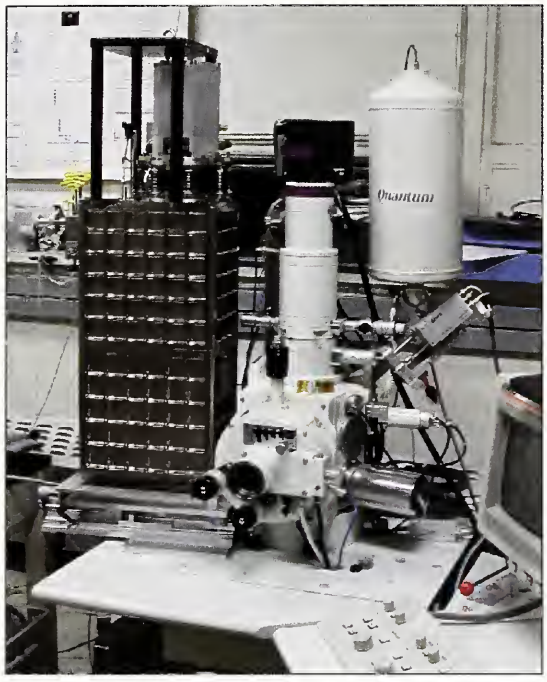

Figure 2. Cryogen-free adiabatic demagnetization refrigerator (left) undergoing vibration testing on a scanning electron microscope.

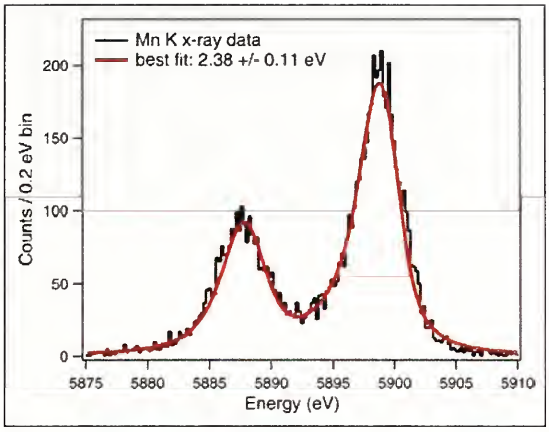

Figure 3. X-ray spectrum from improved NIST microcalorimeter. The FWHM resolution was 2.4 eV for 5.9 keV X-rays.

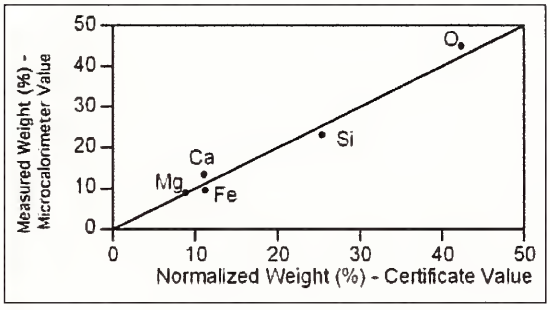

Figure 4. Comparison of elemental weights determined by microcalorimeter with certificate values for NIST K411 standard reference glass. The solid line corresponds to perfect agreement between microcalorimeter and certificate values. (data courtesy of Terry Jach)

■ We recently developed a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated a world record energy resolution of 2.4 eV FWHM at 5.9 keV (see Fig. 3). We also hold the world record for energy resolution for an EDS X-ray detector of 2.0 eV at 1.5 keV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available.

■ We continue to support the microcalorimeter system installed on a CSTL scanning electron microscope in Gaithersburg, Maryland. This year, we provided data analysis support and provided replacement feedback electronics. As shown in Fig. 4, CSTL staff have recently demonstrated the ability of the microcalorimeter to do quantitative microanalysis.

■ We recently demonstrated the ability to read out eight TES microcalorimeters in a single multiplexed amplifier channel with 3.8 eV FWHM energy resolution (Fig. 5). The detectors were fast, having a signal decay-time constant of about 150 microseconds. Combining this result with closed-form calculations and a new Monte-Carle software

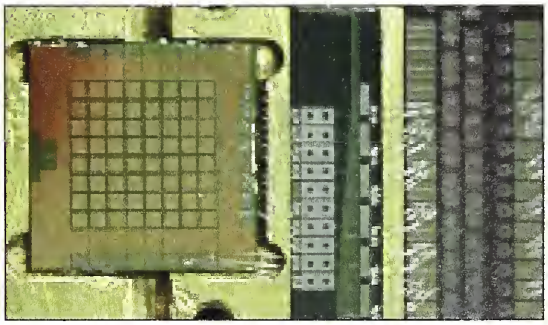

Figure 5. Photograph of an 8x8 array of microcalorimeters. Each microcalorimeter has a 1.5-μm-thick Bi absorber. The middle chip is a filter chip. The chip on the right is a SQUID multiplexer.

package that performs a detailed simulation of our SQUID multiplexer, we can reliability predict the future performance of the multiplexer system. In particular, with only evolutionary improvements to the basic architecture, our time-division SQUID multiplexer will be able to readout 32 detectors per channel with 4 eV resolution or better. Planned improvements include increased open-loop system bandwidth, well-matched pulse rise and fall times, lower SQUID noise, and optimization of the coupling between microcalorimeters and SQUIDs. We have built a test apparatus to house and read out up to 128 microcalorimeter pixels and are preparing to demonstrate multiplexed operation of a 3 x 32 high-resolution microcalorimeter array.

- We have continued work on an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK. If successful, this refrigerator could greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small and inexpensive ^{3}He systems coupled to the solid-state refrigerator. The device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. Recently, we demonstrated refrigerators able to cool bulk material as well as electrically separate pieces of thin-film electronics, such as a X-ray microcalorimeter (Fig. 6). The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. We recently cooled a thin-film payload from 320 mK to 225 mK. This work has been featured twice on the cover of *Applied Physics Letters* and once on the cover of *Physics Today*.

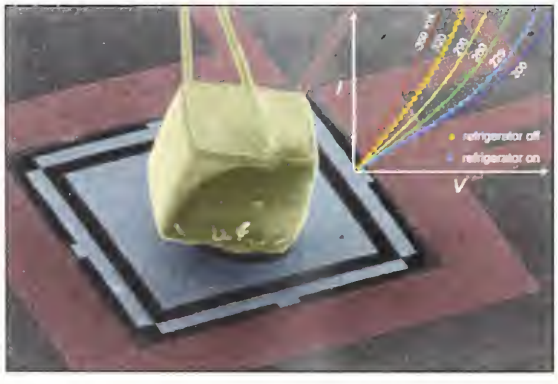

Figure 6. Colorized micrograph of solid-state refrigerator. A cube of germanium (yellow) located on a suspended, micromachined membrane is cooled by four pairs of normal-insulator-superconductor tunnel junctions. The ratio of the volumes of the germanium and the junctions is the same as the ratio of the volumes of the Statue of Liberty and an ordinary person (about 11 000). Macroscopic wires (at upper left) contact the germanium to measure its resistance; these are cooled as well.

- We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 7). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate

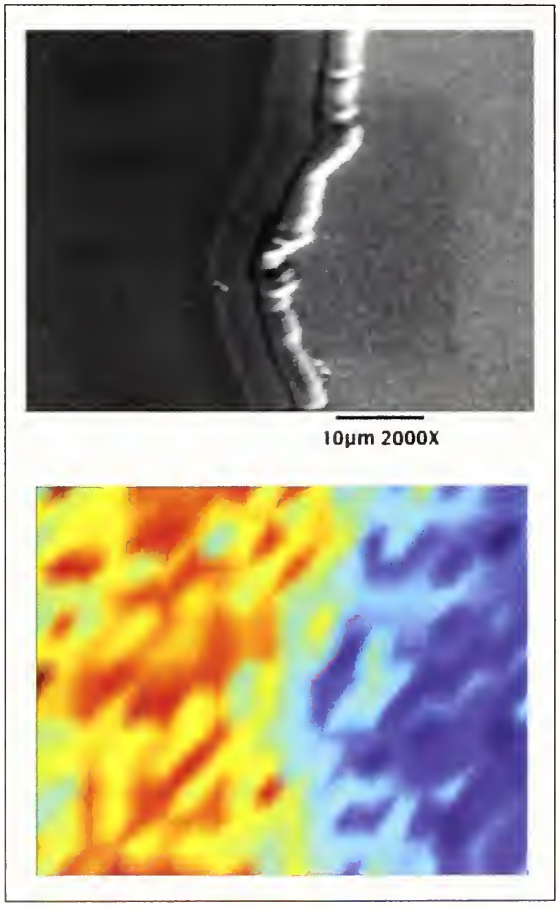

Figure 7. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

Collaborations

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

Recent Publications

J. N. Ullom, J. A. Beall, W. B. Doriese, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, G. C. O'Neil, C. D. Reintsema, L. R. Vale, B. L. Zink, *"Optimization of TES Microcalorimeters,"* accepted, Nuclear Instruments and Methods A (2006).

W. B. Doriese, J. A. Beall, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, C. D. Reintsema, J. N. Ullom, L. R. Vale, Y. Xu, *"Toward Kilopixel Arrays: 3.8 eV Microcalorimeter Resolution in Eight-Channel SQUID Multiplexer,"* accepted, Nuclear Instruments and Methods A (2006).

N. A. Miller, A. M. Clark, D. R. Schmidt, J. A. Beall, G. C. Hilton, K. D. Irwin, L. R. Vale, J. N. Ullom, *"A Practical Electron Tunneling Refrigerator: Cooling of Low Temperature Detectors and Bulk Material,"* accepted, Nuclear Instruments and Methods A (2006).

K. D. Irwin, *"Noise Theory of Nonlinear, Nonequilibrium Calorimeters and Bolometers,"* accepted, Nuclear Instruments and Methods A (2006).

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Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. To this end we have initiated a new program, "Device Design and Characterization." One project that has to be highlighted because it will impact all the projects in the portfolio over time is the Advanced Measurements Nanofabrication Facility Support project. With the completion of the Advanced Measurements Laboratory on the Gaithersburg, Maryland campus, we have populated a cleanroom facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.

Device Characterization and Reliability

Technical Contacts:
J. Suehle
E. Vogel
M. Green

Goals

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, physical models for wear-out, and methodologies to determine energy band diagrams for metal/high-κ systems.

A specific focus is to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (*i.e.*, the gate dielectric, SiO_2, and the gate electrode, doped polycrystalline Si), which has served the industry for 35 years, must now be entirely replaced with one having a higher capacitance and lower power dissipation. Gate dielectrics having higher dielectric constants than SiO_2 will replace SiO_2, and metal electrodes will replace polycrystalline silicon. The enormous complexity of selecting the proper combinations of new gate dielectrics and gate metal electrodes can only be attacked using combinatorial materials methodologies. Therefore, we will be implementing this technology.

Customer Needs

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) with effective thickness values dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal silicates.

Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (*e.g.*, Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy

There are two main focus areas for this project:

- Developing electrical and reliability characterization techniques for ultra-thin SiO_2/oxynitrides and high dielectric constant gate dielectrics.

- Develop combinatorial (fast, local) measurement techniques to measure appropriate electrical properties on gate stacks consisting of new gate dielectric and gate metal electrode materials.

The first focus area is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage, V_t, instability, defect generation rates and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied

to the metal oxide and silicate dielectrics for a variety of high-κ samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

DELIVERABLES:

- Develop ultra-fast current-voltage and "On-the-fly" characterization of charge trapping in High-κ MOSFETs. 2Q 2006
- Use scanning Kelvin probe microscopy (SKPM), CV, and IPE to compare metal work functions of high-κ stacks. 3Q 2006
- Study time-dependent dielectric breakdown in metal gate/high-κ gate dielectric systems. 4Q 2006
- Compare metal work function measurements with measurements performed with other techniques including internal photo emission and scanning Kelvin probe microscopy on ternary metal systems produced by combinatorial techniques. 4Q 2006

Accomplishments

Fundamental Understanding of Metal Gate Workfunction and Barrier Height Measurements using CV analysis

■ C-V measurements were performed on TaN/TaSiC/HfO_2/SiO_2, TaN/TaCN/HfO_2/SiO_2, TaN/TaSiC/SiO_2, and TaN/TaCN/SiO_2 stacks provided by SEMATECH. The HfO_2 films were deposited on a single wafer with a SiO_2 interfacial layer that varied in thickness such that metal workfunction can be obtained by extrapolating the CV flatband voltage to 0 equivalent oxide thickness (EOT). The C-V curves were modeled using the North Carolina State University CVC program, and the workfunction was obtained from the SiO_2 thickness dependence. Figure 1 shows the flatband voltage as a function of EOT on SiO_2. The effective workfunction of 4 nm TaSiN (4.13 eV) is approximately 0.25 eV smaller than that of 4 nm TaCN (4.38 eV). The effective workfunction of these metals on HfO_2 are observed to be ~0.3 eV smaller than on SiO_2. We have performed IPE measurements on all wafers and different thicknesses of SiO_2 stack. We observe numerous transitions and are in the process of performing modeling to understand the results. We have also performed Scanning Kelvin-Probe Microscopy (SKPM) and are in the process of analyzing these data.

Film thickness dependence of

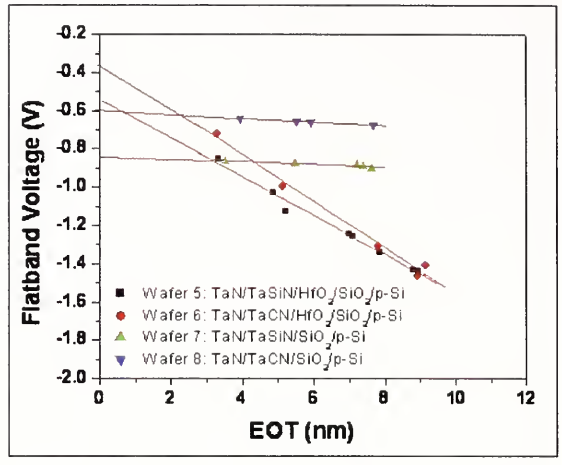

Figure 1. Flatband voltage as a function of EOT to extract effective workfunction for TaN/TaSiC/HfO_2/SiO_2, TaN/TaCN/HfO_2/SiO_2, TaN/TaSiC/SiO_2, and TaN/TaCN/SiO_2 stacks.

Sub-bandgap defect states observed in polycrystalline hafnium oxide

■ We compare hafnium-based high-κ dielectric films grown by MOCVD and atomic layer deposition (ALD). MOCVD-grown HfO_2 films are mostly monoclinic, while HfSiO films are amorphous. Thin ALD-grown HfO_2 films are amorphous, while thick films are monoclinic, with traces of orthorhombic or tetragonal phase present. Figure 2 (page 161) shows that sub-bandgap absorption is observed in polycrystalline, but not in amorphous, films. We note that sub-bandgap states may be the underlying cause for gate leakage via Frenkel-Poole hopping. The addition of Si to HfO_2 reduces the tendency for crystallization, mitigating such issues. However, such sub-bandgap states likely will not be a limiting factor in high-κ based CMOS technologies, since they line up close to the band edge and are therefore not accessible at the low gate voltages employed.

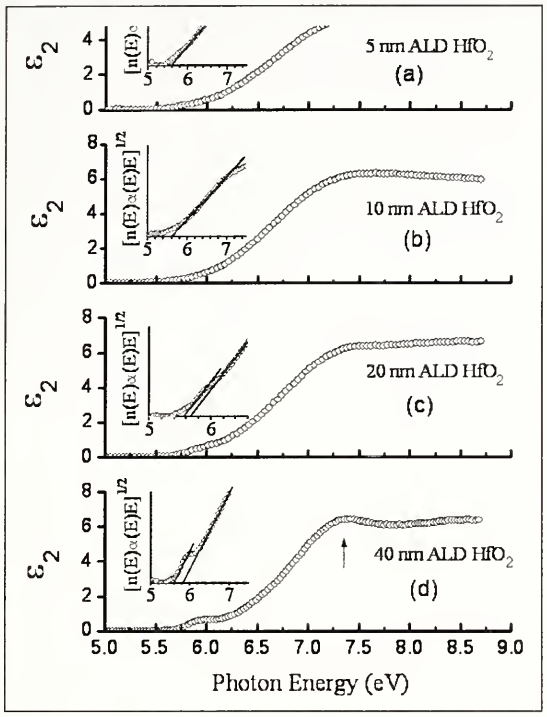

Figure 2. The imaginary part of the dielectric function, determined from VUV-SE data, for 5, 10, 20, 40 nm thick ALD HfO_2 films. All MOCVD HfO_2 spectra (not shown) are similar to that of the polycrystalline 40 nm ALD HfO_2 sample. All MOCVD HfSiO spectra (not shown) are similar to that of the amorphous 5 nm ALD HfO_2 sample.

Optimization of Scanning Kelvin Probe Microscopy for determining metal work function

■ A series of modifications and optimizations were performed with the SKPM methodology to improve the determination of metal work function for a variety of different metal samples prepared at NIST. The work function of the PtIr5 probe tip was corrected (4.9 eV) from contact potential measurements performed on specially prepared samples. The initial assumption for the work function of n+-Si was recalculated based on the actual SKPM tip resistivity. Finally, the cleaning of the metal samples was optimized using acetone, methanol, HF, and DI H_2O. The results are shown in Fig. 3. The figure shows the extracted metal work functions for a variety of metals and compared to literature values obtained from different contact potential difference techniques. The agreement is very good as indicated.

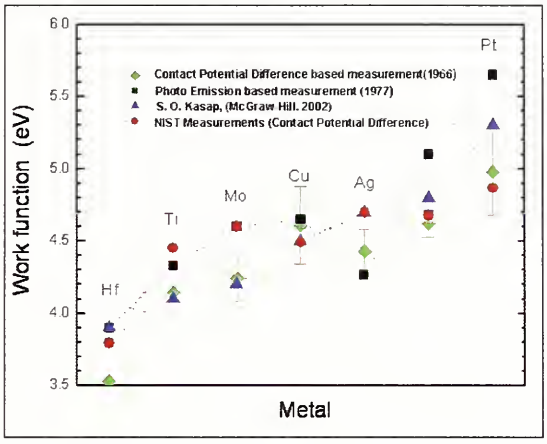

Figure 3. Plot of metal work function determined by Scanning Kelvin Probe Microscopy for seven different metals samples prepared at NIST. The figure shows the comparison with literature values.

Combinatorial Study of Ni-Ti-Pt Ternary Metal Gate Electrodes on HfO_2 for Advanced Gate Stacks

■ Combinatorial techniques were used to study the Ni-Ti-Pt ternary metal gate system deposited on HfO_2 dielectrics. The flat-band voltage (ΔV_{fb}) and leakage current (J_L) were systematically studied through capacitance – voltage (C-V) and current – voltage (I-V) analysis. Both parameters offer a basis for understanding the gate stack properties since they are directly related to the effective work metal work function (Φ_m). A Si shadow-mask with hundreds of nominal 250 μm^2 openings was placed directly on top of the wafer to make in-situ metal-oxide-silicon capacitors (MOSCAPS). Capacitance-voltage and current-voltage data were obtained by measuring a combinatorial array of several hundred capacitors. Figure 4 shows a two-dimensional map of ΔV_{fb} (extracted from CV analysis) and J_L. A more negative ΔV_{fb} is observed close to the Ti-rich corner than close to the Ni- and Pt-rich corners. This observation implies a smaller

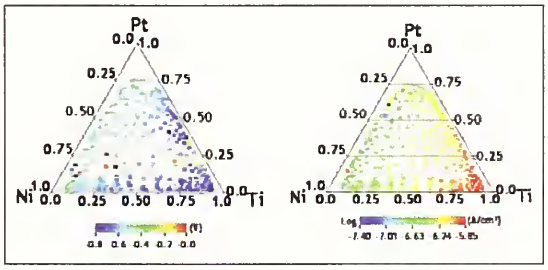

Figure 4. shows the map of the flat-band voltage shift (ΔV_{fb}) extracted from C-V characteristics at 1 kHz across the Ni-Ti-Pt libraries (left plot)and the leakage current density (J_L) map measured at an applied D.C. substrate bias of -1 V (right plot).

Φ_m near the Ti-rich corners and higher Φ_m near Ni- and Pt-rich corners. In addition the measured J_L values are consistent with the observed ΔV_{fb} variations.

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

Professional Committee Participation

Technical Chair, IEEE International Reliability Physics Symposium (J. Suehle)

Technical Chair, IEEE Interface Specialist Conference (E. Vogel)

Management Committee, IEEE International Integrated Reliability Workshop (J. Suehle)

Technical Committee, IEEE International Electron Device Meeting (J. Suehle)

SEMATECH/SIA working committees (E. Vogel)

Collaborations

IBM, Alternative Gate Dielectrics

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Lucent Technologies, Reliability Characterization of ultra-thin gate dielectrics.

SEMATECH Characterization of metal gate high-κ systems.

Rutgers University, Characterization of high-κ gate dielectrics

University of Maryland, College Park, ultrathin gate oxide reliability

U. Texas at Austin, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics

Recent Publications

D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, G. Bersuker, P. Y. Hung, and A. Diebold, *"Electrical Characterization of Spatial Distributions of Trapping Centers in HfO_2/SiO_2 Gate Stack,"* submitted to IEEE Trans. Elec. Dev. (submitted for press).

S.-E. Park, J. S. Suehle, J. J. Kopanski, E. M. Vogel, and A. Davydov, *"Determination of work functions for metals by scanning Kelvin probe microscopy,"* submitted to J. Appl. Phys. (submitted for press).

D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, P. Y. Hung, and A. Diebold, G. Bersuker, *"Spatial Distributions of Trapping Centers in HfO_2/SiO_2 Gate Stacks,"* accepted Appl. Phys. Lett. (submitted for press).

J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold, *"A Comparison of Thickness Values for Very Thin SiO_2 Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements,"* Journal of the Electrochemical Soc., vol. 153, p. F12 (2006).

S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, *"Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures,"* J. Vac. Sci Tech. B, vol. 24, p. 404 (2006).

S.-E. Park, J. S. Suehle, J. J. Kopanski, and E. M. Vogel, *"Calibration of work function for Pt0.95Ir0.05 films with scanning Kelvin probe microscopy,"* Appl. Phys. Lett., 88, on-line, (2006).

N. V. Nguyen, D. Chandler-Horowitz, A. Davydov, C. Hacker, S. Park, H. Xiong, J. Ehrstein, J. Kopanski, J. Suehle, E. Vogel and M. Frank., *"Crystallinity and Defects in Hafnium Oxide and Hafnium Silicate Films,"* "High Dielectric Constant Gate Stacks III," of the 208th Meeting of The Electrochemical Society in October 16-21, 2005.

D. R. Burgess, Jr., J. E. Maslar, W. S. Hurst, E. F. Moore, W. A. Kimes, R. R. Fink, N. V. Nguyen, *"Atomic Layer Deposition – Process Models and Metrologies,"* AIP Conference Proceedings 788, Characterization and Metrology for ULSI Metrology Technology, pp. 69-72, (2005).

S. Sayan, M. Croft, N.V. Nguyen, T. Emge, J. Ehrstein, I. Levin, J. Suehle, R.A. Bartynski, E. Garfunkel, *"The relation between crystalline phase, electronic structure, and dielectric properties in high-κ gate stacks,"* AIP Conference Proceedings 788, Characterization and Metrology for ULSI Metrology Technology, pp. 92-101, (2005).

J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, and J. S. Suehle, *"Reverse Short Channel Effects in High-κ gated nMOSFETs,"* Microelectronics Reliability, vol. 45, p. 783, (2005).

(Invited) J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein, *"Detailed Study and projection of Hard Breakdown Evolution in Ultra-thin gate Oxides,"* Microelectronics Reliability, 45, p. 419 (2005).

N. V. Nguyen, Albert V. Davydov, D. Chandler-Horowitz, M. M. Frank, *"Sub-bandgap defect states in polycrystalline hafnium oxide and their suppression by admixture of silicon,"* App. Phys. Lett. 87 (2005).

N. V. Nguyen, S. Sayan, I. Levin, J. R. Ehrstein, I. J. R. Baumvol, C. Diremeier, C. Krug, L. Wielunski, P. Y. Hung, and A. Diebold, *"Optical band gaps and composition dependence of hafnium-aluminate thin films grown by atomic layer chemical vapor deposition,"* J. Vac. Sci. Technol. A 23 (2005).

S. Sayan, N. V. Nguyen, and J. Ehrstein, T. Emge and E. Garfunkel, I. Levin, E. P. Gusev, H. Kim and P. J. McIntyre, *"Structural, Electronic, and dielectric properties of ultrathin zirconia films on silicon,"* Applied Physics Letter 86, 152902 (2005).

S. Sayan, N. V. Nguyen, and J. Ehrstein, J. J. Chambers, M. R. Visokay, M. A. Quevedo-Lopez, L. Colombo, D. Yoder, I. Levin, and D. A. Fischer, M. Paunescu, O. Celik, and E. Garfunkel, *"Effect of nitrogen on band alignment in HfSiON gate dielectrics,"* Appl. Phys. Lett. 87, 212905 (2005).

Park, S., Kopanski, J. J., Kang, Y. , Robins, L. H., *"Surface photovoltage spectroscopy of minority carrier diffusion lengths in undoped and Si-doped GaN epitaxial films,"* Physica Status Solidi, (24-MAR-2005).

Nanoelectronic Device Metrology

Technical Contacts:
C. Richter
N. Zimmerman
A. Davydov

Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable new nanotechnologies (such as Si-based quantum devices and molecular electronics) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. Two related goals are the optimization of Si-based single-electron devices for one-electron logic, and the development of ultra-sensitive nanotransistor devices to observe charge reconfigurations in biological systems. Another targeted goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably (see Fig. 1).

Figure 1. Curt Richter loads a molecular electronic sample for electrical characterization.

Customer Needs

Mainstream CMOS, which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is approaching fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) (http://public.itrs.net/) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approaeh are molecular electronics and Si-based quantum electronic deviees. Moleeular eleetronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Finally, there is a large potential set of customers for ultra-sensitive charge electrometry of biological systems. Many diseases result from changes in protein structure or folding. We will investigate whether such changes can be elucidated through capacitive coupling to nearby nanotransistors.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Beeause these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

Technical Strategy

Develop the electrical and physical metrology of Si-based nanoelectronics. The focus is on the basic building bloeks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined (see Fig. 2).

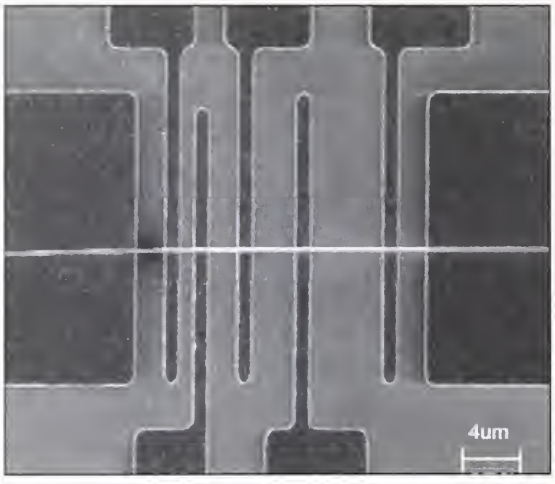

Figure 2. A silicon nanowire grown by chemical vapor deposition integrated into a transfer length method test structure to determine nanowire contact resistance.

DELIVERABLES:

- Complete investigation of two-dimensional electrostatics in dual-gated Si-nanowire FETs nanofabricated from SOI wafers; prepare and submit manuscript. 4Q 2005
- Complete development of a simple single nanowire manipulating system (SNMS) to precisely transfer and align individual nanowires into test structures for electrical characterization; prepare and submit manuscript. 3Q 2006

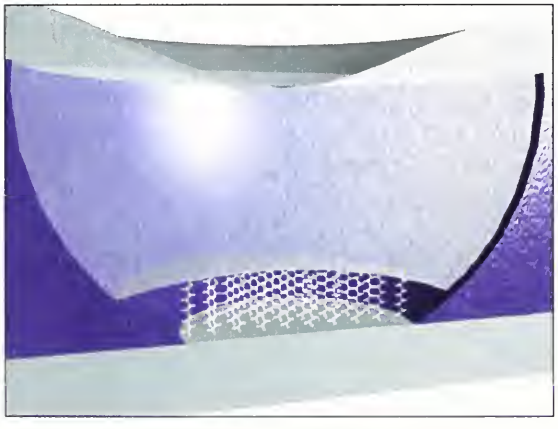

Figure 3. Schematic overview of a suspended Si_xN_y membrane nanopore-based molecular electronic test structure.

Develop robust molecular test structures (see Fig. 3, for example) in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models.

DELIVERABLES:

- Develop, demonstrate, and disseminate a novel FTIR-based technique to characterize top-metal/molecular interfaces. Investigate initial metal/molecule interfaces. Prepare and publish manuscript. 4Q 2005
- Utilize backside FTIR-based technique to characterize top-metal/molecular interfaces, and investigate metal/molecule interactions. Prepare and submit manuscript. 3Q 2006
- Assess the ability of Si_xN_y membrane nanopore-based molecular electronic test structures to characterize spin-dependent inelastic tunneling processes in molecular magnetic tunnel junctions – devices that combine features of moletronics and spintronics. Prepare and submit manuscript. 3Q 2006

Develop geometries and architectures that maximize flexibility and operating temperature of single-based single-electron devices.

DELIVERABLES: Complete and publish an experimental and theoretical study comparing charge offset drift in metal-based and Si-based SET transistors and/or the static charge offset problem in Si-based SET transistors. 4Q 2005

Determine the ultra-sensitive charge electrometry capabilities of Si-nanotransistors through measuring the sensitivity and its relationship to device structure. A longer term strategy is to assess how the sensitivity is affected by biological structures in solution.

DELIVERABLES: Develop a "nano-gap capacitor" to characterize electrical breakdown in air at small separations. 2Q 2006

Develop measurement methodology, models, and understanding needed to apply Scanning Capacitance Microscopy (SCM) and Scanning Kelvin Force Microscopy (SKFM) to the quantitative measurement of the local electrical properties of nanowires and other nanoelectronic devices. Probe shape, probe metal, operating conditions, and sample surface properties all influence the measured contact potential difference with SKFM. The accuracy of the measurement can be improved by careful control of the measurement properties, use of reference materials, and modeling (see Fig. 4).

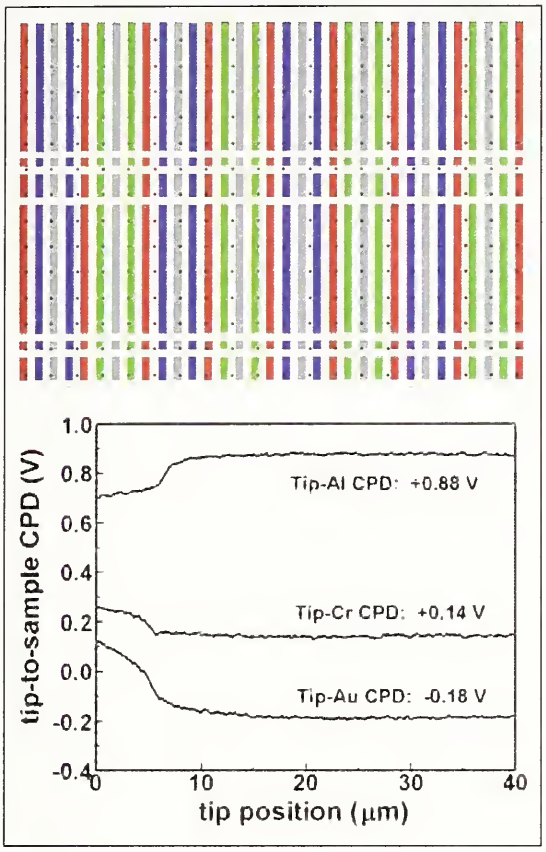

Figure 4. Top: Simulated nanowire test structure consisting of four distinct metal lines in various repeat patterns. Bottom: Initial SKFM characterization of Kelvin Probe workfunction and resolution test structure. Measured work functions agree to within 90 mV of handbook values. Nanostructures introduce complicating geometry and surface effects.

DELIVERABLE: Determine the limitations and best possible accuracy of the SKFM measurement of surface potential when applied to nanowires. Apply SCM and SKPM to the measurement of the electrical properties of nanostructures, such as dopant concentration, work function, and surface state density.
4Q 2006

Accomplishments

■ *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated.* Dr. Sang-Mo Koo and colleagues have demonstrated that silicon nanowire (SiNW) field effect transistors (FETs) fabricated by a standard 'top-down' approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel (1000 cm^2/Vs) is found to be two times higher than that of the reference MOSFET of large dimension (W >1 μm). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today's standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors.* We have shown that SiNWs with Schottky contacts can be used as enhancement-mode FETs with an excellent on/off current ratio. The process does not require any source and drain doping or silicide formation, thereby allowing for a simple process without thermal annealing. Silicon nanowire field-effect transistors (SiNWFETs) were fabricated with a highly simplified integration scheme to function as Schottky barrier transistors with excellent enhancement-mode characteristics and a high on/off current ratio ~10^7. SiNWFETs show significant improvement in the thermal emission leakage (~6×10^{-13} A/μm) compared to reference FETs with a larger channel width (~7×10^{-10} A/μm). The drain current level depends substantially on the contact metal work function as determined by examining devices with different source-/drain- contacts of Ti (≈4.33 eV) and Cr (≈4.50 eV). The different conduction mechanisms for accumulation- and inversion-mode operation were determined and confirmed by comparison with two-dimensional numerical simulation results. Schottky barrier FETs are of great interest in their own respect as an alternative to traditional doped source and drain device structure, because sub-100 nm range scaling encounters fundamental problems including high leakage current and parasitic resistance. Schottky barrier FETs have a number of advantages including simple and low-temperature processing, good suppression of short-channel effects, and the elimination of doping and subsequent activation steps. These features are particularly desirable for SiNW devices because they can circumvent difficult fabrication issues such as an accurate control of the doping type/level and the formation of reliable ohmic contacts (see Fig. 5, page 168).

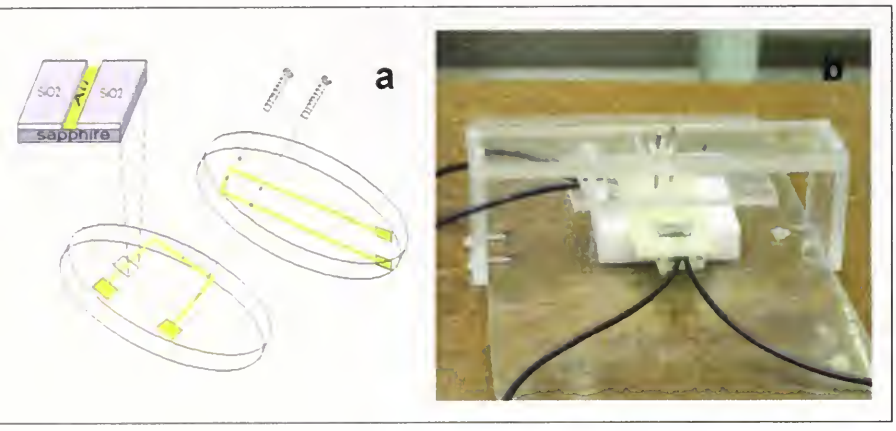

Figure 5. Assembly drawing and photograph of our nano-gap capacitor.

■ *Two-dimensional Electrostatics to Enhance Channel Modulation in Dual-gated Silicon Nanowire Devices.* We have experimentally observed enhanced channel modulation in dual-gated silicon nanowire (SiNW) field-effect transistors (FETs). In this work, SiNW FETs were fabricated using electron-beam lithography to investigate the electrostatic control of current in semiconductor nanowire devices. These novel top- and bottom-gated FETs are based upon simple top-down test structures that rely upon self-aligned Schottky-contacts to enable the electronic properties of SiNWs to be readily studied. Improved device performance is observed for the dual-gated SiNW FETs when compared to simultaneously fabricated large area control FETs. The SiNW devices (with widths down to approximately 60 nm) exhibit an on/off current ratio greater than 10^6, which is more than three orders of magnitude higher than that of control devices prepared simultaneously having a large channel width (5 μm). In addition, the top gate is found to suppress ambipolar conduction effectively, which is one of the factors limiting the use of nanotube or nanowire FETs for complimentary logic applications. Two-dimensional numerical simulations have confirmed an important physical insight illustrated by this work: due to the reduced dimensionality of SiNWs, electrostatic control is enhanced when compared to larger channel width devices.

■ *Comparison of charge offset drift in metal-based and Si-based SET transistors.* We have completed a study comparing the charge offset drift in metal-based and Si-based SET transistors. To date, there has been no reproducible way to eliminate the charge offset drift in metal-based SET devices, while Si-based devices have been characterized that exhibited minimal charge offset drift. The long-term charge offset behavior appears to be correlated with an observation in the short-term noise: two-level fluctuators in the Si-based devices are completely stable with respect to time, thermal cycling, etc.; in contrast, two-level fluctuators in the metal-based devices are notoriously "fragile." We have devised a model that comprehensively explains these results: in the metal-based devices, the defects that produce the drift are interacting strongly, as if they are in a glassy environment. These interactions are the underlying source of the long-term drift, and of the lack of stability in individual two-level fluctuators. This analysis leads us to suggest that a new fabrication process in which the metal films are deposited with low stress will improve the performance of the metal-based devices.

■ *Nano-gap capacitors.* We have succeeded in devising an assembly process and measurement scheme that allows us to measure the electrical breakdown in air with greater accuracy than previously reported. This new capability depends crucially on the ability to accurately measure the gap, which we accomplish by a combination of capacitance measurements and simulations of capacitance versus separation. We have shown the ability to measure over a range of separations between 0.3 microns and 50 microns. These measurements of electrical breakdown in air at small separations are of increasing importance to the MEMS field.

We have also investigated the standard theory for the breakdown at small separations (below about 5 microns). In this regime, the standard theory uses Fowler-Nordheim tunneling in vacuum, along with a surface roughness-induced field enhancement; this field enhancement is typically a factor of about 100. By combining electrical breakdown measurements with AFM measurements of surface roughness, we have for the first time been able to quantitatively test this theory. We find that the roughness in our smooth Au films is much smaller than necessary for the standard theory to be correct. We conclude that the standard theory cannot explain our experiments, and by extension is suspect in most of the measurements done to date.

■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements.* Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nano-

technology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental setup. Electrical (current-voltage, or IV) measurements of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of molecular electronic devices are often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what well may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Novel approach to investigate buried metal-organic interfaces for molecular electronics*. We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples as prepared encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance. Two different chemical processes were utilized to attach nm-thick alkane films to the Si substrates: a conventional silanization process for films on thin oxides and a novel process previously optimized at NIST for direct attachment to silicon. Molecules on silicon are of interest as active electronic layers and for surface engineering. Monolayers bound directly to silicon are expected to have less interfacial capacitance than those on oxides, be more amenable to further processing, and be resistant to degradation die to the nature of the strong covalent bond. Results were presented at the 7th International Molecular Electronics conference and published.

FY Outputs

Collaborations

NTT, Akira Fujiwara, Si-nanowire metrology

Hewlett-Packard, R. Stanley Williams et al., Interface properties of molecular electronic test structures

NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures

Recent Publications

Fujiwara, A. F, I. Hiroshi, K. Yamazaki, H. Namatsu, Y. Takahashi, N. M. Zimmerman, S. B. Martin, *"Single electron tunnelling transistor with tunable barriers using silicon nanowire MOSFET,"* Appl. Phys. Lett. 88, 053121 (30-JAN-2006).

Hourdakis, E., B. J. Simonds, N. M. Zimmerman *"Sub-micron gap capacitor for measurement of breakdown voltage in air,"* Rev. Sci. Instr. 77, 034702 (MAR-2006).

Koo, S. M., Q. L. Li, M. D. Edelstein et al., *"Enhanced channel modulation in dual-gated silicon nanowire transistors,"* Nano Letters 5 (12), 2519 (DEC-2005).

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Richter, C. A., D. R. Stewart, D. A. A. Ohlberg, R. S. Williams; *"Electrical Characterization of Al/AlO$_x$/Molecule/Ti/Al Devices,"* Appl. Phys. A 2005, 80, 1355–1362. (March 2005).

Hacker, C. A.; Anderson, K. A.; Richter, L. J.; Richter, C. A.; *"Comparison of Si-O-C interfacial bonding of alcohols and aldehydes on Si(111) formed from dilute solution with ultraviolet irradiation,"* Langmuir 21(3), 882-889 (2005).

Koo S.-M., A.-F. Fujiwara, J.-P. Han, E. Vogel, C. Richter, and J. Bonevich, *"High Inversion Current in Silicon Nanowire Field Effect Transistors,"* Nano Lett., Vol. 4, 2107-2111, Nov. 2004.

Richter L. J., C. S. Yang, P. T. Wilson, C. Hacker, R. D. van Zee, J. J. Stapleton, D. L. Allara, J. M. Tour, *"Optical Characterization of Oligo(phenylene-ethynlyene) Self-Assembled Monolayers on Gold,"* J. Phys. Chem. B., Vol. 108, No. 33, pp. 12547-12559 (19-AUG-2004).

Hacker C. A., J. D. Batteas, J. C. Garno, M. Marquez, C. A. Richter, L. J. Richter, R. D. van Zee, C. D. Zangmeister, *"Structure and Chemical Characterization of Self-Assembled Mono-Fluoro-Substituted Oligo(phenylene-ethynlyene) Monolayers on Gold,"* Langmuir, Vol. 20, No. 15, pp. 6195-6205 (22-JUN-2004).

Richter C. A., C. Hacker, L. J. Richter, E. M. Vogel, *"Molecular Devices Formed by Direct Monolayer Attachment to Silicon,"* Solid State Electronics, Vol. 48, pp. 1747-1752 (17-JUN-2004).

Power Semiconductor Device Metrology

Goals

The goal of the project is to develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices.

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient power generation, transmission and distribution. Rapid technical advances are occurring in the development of new power semiconductor materials and designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize industry and military power distribution and conversion by extending the use of switch-mode power conversion technology, with its superior efficiency and control capability, to high voltage applications.

"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems."

Several industry and government programs are currently underway to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently announced WBST-HPE Phase 3 effort (http://www.darpa.mil/baa/baa06-30.html) anticipates that this semiconductor technology will enable the HV-HF switching required for a Solid State Power Substation (SSPS). The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements. In addition the Department of Energy has identified HV-HF power devices as an enabling technology for alternative energy sources and energy storage systems.

Technical Strategy

The NIST strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of power devices and ICs. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters to aid in application insertion. NIST is taking a lead role in developing the device metrology and performance metrics necessary for industry and government HV-HF semiconductor device development efforts.

Support Programs to Develop HV-HF Semiconductor Devices and Applications

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. Conventional distribution approaches being considered for the next generation of aircraft carriers employ a 13.8 kV a.c. power distribution that is stepped down to 465 V a.c. by

Technical Contact:
A. Hefner

using large (6 ton and 10 m^3) 2.7 MVA transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2 and 3 programs for 2005 through 2008.

DELIVERABLES: Participate in planning future government and industry high power generation, transmission, and distribution programs enabled by emergence of HV-HF power semiconductor devices including WBST-HPE Phase 3, EPRI Intelligent Universal Transformer Program, and the DOE Fuel Cell Power Plant program. 3Q 2007

Metrology High-Voltage High-Frequency Switching Device Performance

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester, c) 3 kV 30 A 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter module package measurement system, and f) rapid thermal cycling/shock module package stress system.

DELIVERABLES: Apply NIST high-voltage, high-frequency power device test systems to evaluate the performance the 10 kV, 100 A, 50 ns half-bridge power modules produced by the DARPA WBST-HPE program and asses the potential for enabling advance commercial and military power distribution systems. 1Q 2007

Metrology for SiC Device Degradation and Reliability

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for bipolar-type devices (devices with minority carrier injection) is the degradation in the electrical characteristics after prolonged forward bias conduction. The degradation occurs from latent material defects such as Basel Plane Dislocations that result in the formation and growth of stacking faults activated by excess-carrier recombination. NIST has recently developed automated stress and degradation monitoring systems to assess degradation of SiC devices. The monitoring methods include forward conduction voltage drop, switching reverse recovery characteristics, and pulsed thermal imaging of current uniformity.

DELIVERABLES:

- Use NIST forward-bias stress and degradation monitoring systems to assess progress of WBST-HPE program in producing degradation-free PiN diodes using Low Basel Plane Dislocation Density epitaxial layer technology. 3Q 2006
- Develop a long term application-like 20-kHz switching test system to evaluate HV-HF application reliability and use to evaluate reliability of DARPA WBST-HPE. 1Q 2007

SiC Power Device Models for HV-HF Power Converter Simulation

Accurate and robust circuit simulator models for HV-HF semiconductor devices are needed to evaluate the impact of the new semiconductor technology on power converter system performance. NIST develops the generic physics-based models for the SiC power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods needed to measure the physical and structural parameters of specific devices. The NIST model parameter extraction tools have recently been used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 program resulting in models that were used to predict the performance of the Phase 3 SSPS.

DELIVERABLES: Collaborate with industry and government programs to simulate the performance of HV-HF devices in power conversion system applications. 4Q 2007

Accomplishments

■ *NIST played a key role in planning and coordinating government and industry programs and activities on high voltage SiC power devices including:* Evaluated contractor performance for DARPA WBST HPE Phase 2. Participated in planning and writing BAA for DARPA WBST HPE Phase-3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day. Served as Member of DARPA/ONR SSPS Government Independent Design Panel.

Participated in planning ONR Mantech SiC Power Device manufacturability program. Served as panel member for DOE Program on SiC-based Inverters in Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. Participated in planning U.S. Army TACOM program on Reliable 4H-SiC MOSFET for Hybrid Electric Vehicle Power Systems. Served as the Moderator for the SiC Devices and Materials Focus at the DARPA/ONR Future of Power Electronics Workshop and assisted in determining the focus for a future DARPA SiC power device program. Served as the Chairman for the Industrial News Session at the International Conference on Silicon Carbide and Related Materials. Served as a reviewer for the DOE FreedomCAR and Vehicle Technologies Programs.

■ *NIST unique HV-HF device metrology demonstrated unprecedented performance of DARPA WBST-HPE:* The NIST high voltage curve tracer and the NIST high-voltage high-frequency (HVHF) switching test systems were used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs, *e.g.*, 10 kV, 12 A, 50 ns inductive load switching. Typical high voltage silicon devices require several microseconds to switch. Significant advances in materials, device design and HV-HF metrology were required for this achievement.

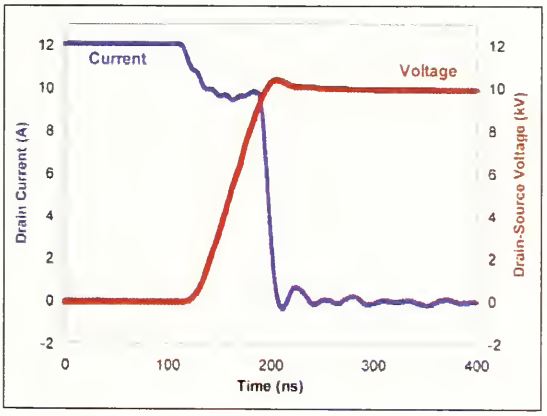

Figure 1. NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A and 200 °C in less than 100 ns. High voltage silicon power devices require several microseconds to switch even at half the voltage and 125 °C. These devices were produced by Cree Inc under the DARPA WBST-HPE Phase II program.

■ *NIST HV-HF SiC models were used to simulate system performance:* NIST's metrology, device modeling, and parameter extraction tools have resulted in software models for the HV-HF devices that are being produced by the DARPA WBST HPE program. These models are being used by industry and government to simulate the performance of future power distribution and conversion systems enabled by the new HV-HF semiconductor device technology.

■ *High voltage clamped inductive and resistive switching test bed developed.* A low parasitic inductance 15 kV switching test system for clamped inductive and resistive SiC MOSFET switching characterization was developed and integrated into the 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 20 kV voltage isolation and 350° C maximum controllable temperature was also included to enable investigation of HV-HF device characteristics at elevated operating temperature.

■ *Extended capabilities of IMPACT parameter extraction software.* The capabilities of the parameter extraction software, IMPACT, were extended to include MOSFETS (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). The parameter extraction hardware was also extended to enable capacitance versus gate- and drain-voltage characterization up to 5 kV.

■ *NIST determined that the SiC PiN diode forward bias degradation due to stacking fault growth is also accompanied by reduced reverse recovery charge and by substantial reduction in device conduction area.* This is significant because it was shown that a factor of ten reduction in conduction area and thus current handling capability occurs for what was previously thought to be a small increase on-state voltage. The paper describing this work won the William M. Portnoy Award at the IEEE 39th Annual Meeting of the Industry Applications Society in October 2004.

Collaborations

Synopsys Inc., SiC power device modeling and parameter extraction for IGBT library component models

CREE, Characterization and application of SiC power devices

Northrop Grumman Corp., Characterization and application of SiC power devices

Virginia Tech., Silicon and SiC power device utilization

Powerex, Power semiconductor device packaging

DARPA/ONR/Navsea, SiC power devices for SSPS and other applications

GE CRD, SiC power devices for robust integrated power electronic systems

University of Puerto Rico Mayagüez, Electro-thermal simulation of power electronic systems

University of Wisconsin Madison, SiC power system simulation

Purdue University/Carnegie Mellon University/Vanderbilt University/Auburn University, Development of process technologies for SiC power devices

Electric Power Research Institute, power semiconductor devices for solid state intelligent universal transformer

Department of Energy, electric vehicle power electronics and power converters for 300 MW fuel cell generation plant

Recent Publications

A. R. Hefner, *"Status of High-Voltage, High-Frequency Silicon-Carbide Power Devices,"* GomacTech 2006, pp. 232-235, (22-MAR-2006).

A. R. Hefner, D. Berning, and C. Ellenwood, *"Metrology For High-Voltage, High-Speed Silicon Carbide Power Devices,"* GOMACTech 2005, pp. 226-229 (2005).

J.-S., Lai, H. Yu, J. Zhang, P. Alexandrov, Y. Li, J. H. Zhao, K. Sheng, K., A. Hefner, *"Characterization of normally-off SiC vertical JFET devices and inverter circuits,"* IEEE Conference Record Industry Applications Society Annual Meeting Volume 1, Oct. 2005, pp. 404-409 (2005).

J. R. Reichl, J.-S. Lai, A. R. Hefner, T. R. McNutt, D. Berning, *"Inverter Dynamic Electro-Thermal Modeling and Simulation with Experimental Verification,"* IEEE Power Electronics Specialists Conference, pp. 2208-2215 (June 2005).

T. R. McNutt, A. R. Hefner, H. A. Mantooth, Jr., J. Duliere, D.W. Berning, R. Singh, *"Silicon carbide PiN and merged PiN Schottky power diode models implemented in the Saber circuit simulator,"* IEEE Transactions on Power Electronics, Volume 19, Issue 3, pp. 573-581 (May 2004).

S. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, A. R. Hefner, *"10 kV, 123-m/spl Omega//spl middot/cm/sup 2/ 4H-SiC power DMOSFETs,"* IEEE Electron Device Letters, Volume 25, Issue 8, pp. 556-558 (Aug. 2004).

J. M. Ortiz-Rodriguez, A. R. Hefner, D. Berning, M. Volez-Reyes, M. Hernindez-Mora, G. Gonzalez, *"Lumped-parameter thermal modeling of an IPEM using thermal component models,"* IEEE Proceedings on Computers in Power Electronics Workshop, pp. 43-48 (Aug.2004).

J. Reichl, D. Berning, A. R. Hefner, J.-S. Lai, *"Six-pack IGBT dynamic electro-thermal model: parameter extraction and validation,"* IEEE Applied Power Electronics Conference and Exposition, Volume 1, pp. 246-251 (2004).

A. Hefner, T. McNutt, A. Akuffo, R. Singh, C. Ellenwood, D. Berning, M. K. Das, J. J. Sumakeris, R. Stahlbush, *"Characterization of SiC PiN diode forward bias degradation,"* IEEE Conference Record Industry Applications Society Annual Meeting Volume 2, pp. 1252-1260 (Oct. 2004).

R. Singh, A. R. Hefner, Jr., *"Reliability of SiC MOS Devices,"* Journal of Solid-state Electronics, Vol. 48, No. 10-11, pp. 1717-1720 (24-JUNE-2004).

Organic Electronics Metrology

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Goals

Organic electronic devices are increasingly being incorporated into electronics packaging and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need exists for new diagnostic probes, tools, and methods to address new technological challenges. Their adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of measurement methods to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provides the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics.

Customer Needs

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high-volume manufacturing, incorporation on flexible substrates, and designed functionality (Fig. 1). Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags. Market estimates range from $10–30 B globally by 2010–2015, with applications in displays, logic, and lighting. Organic light emitting diodes for displays and lighting represent the first products, projected to grow from approximately $0.5 B today to $3 B in 2010. Market expansions to $250 B by 2025 have been estimated should major technology and business barriers be overcome. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

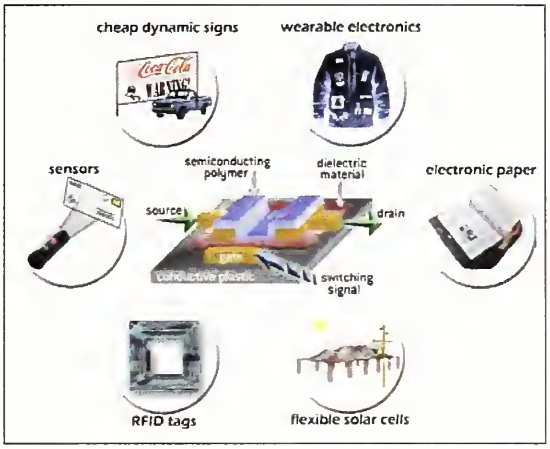

Figure 1. Schematic representation of potential organic electronics applications.

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. Without this knowledge, guided improvements in materials and processing design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces found in organic devices is critical to proper interpretation of charge transport through molecules rather than single crystal structures. Identifying individual contributions to performance variations requires metrology unavailable to device manufacturers and spanning multiple disciplines: device physics, material electronic structure, chemistry, and materials science.

Technical Strategy

The initial focus of the NIST program is on the organic field effect transistor (OFET) because, as in the silicon industry, the transistor is the basic building block for active devices. The fundamental framework, characteristics, and issues that arise during OFET development are transferable to other organic electronic devices because of commonalities in architecture and interfaces. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics: (1) unique measurements of organic materials and interfaces for both (a) structure and chemistry and (b) electronic properties; and (2) the development of an integrated measurement test platform to correlate device performance with the structure and properties of active organic materials.

1. Interfacial structure and chemistry fundamentals: The basic OFET consists of thin layers (30 nm to 60 nm thick) of disparate materials including the organic semiconductor, dielectric, interconnect, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance.

We are developing a suite of powerful measurement methods including X-ray, neutron, and optical probes capable of *in-situ* nondestructive characterization of critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET device evaluation. Near-edge X-Ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements, measure the orientation of interfacial molecules, and quantify film defect levels. Second order nonlinear optical spectroscopies, such as sum frequency generation (SFG) or coherent anti-Stokes Raman spectroscopy (CARS), are particularly appropriate for probing the buried semiconductor/dielectric interface. Interfacial structure (width, roughness) between OFET layers must also be measured in order to interpret performance variations. X-ray and neutron reflectometry are powerful thin film characterization methods for determination of the interfacial profile between layers. Additional information about the materials is obtained using atomic force microscopy (AFM), spectroscopic ellipsometry, and polarized infrared absorption measurements (IR).

DELIVERABLES:

- Complete NEXAFS measurements of evaporated small molecules onto silicon surfaces as a function of film thickness and deposition temperature. 4Q 2005
- NEXAFS measurements of chemical conversion, molecular orientation, and defect density of thermally convertible oligothiophenes with varying number of repeat units. 1Q 2006
- Complete measurements of annealing temperature effects on the thin film morphology of liquid crystalline poly(thiophene) materials. 3Q 2006
- Complete correlation of interfacial structure and transistor performance of liquid crystalline poly(thiophene) materials. 4Q 2006

2. Electronic property fundamentals: The response of organic electronic materials to electrical fields must also be measured to separate device architecture artifacts and intrinsic material properties. Model sandwich test structures have been designed to individually test the frequency response of semiconducting and dielectric materials employed within organic electronic ensembles. Capacitance and conductance measurements will be performed at frequencies up to 12 GHz to determine the dielectric properties of these materials. These results will be compared with traditional metrics such as current or capacitance versus voltage curves as functions of temperature, layer thickness, or contact metals. With new information (electronic and interfacial), we will elucidate mechanisms underlying the many anomalous phenomena observed in OFETs, such as permanent bias instability and the true nature of carrier mobility distribution, both of which are opaque to traditional metrics.

DELIVERABLES:

- Construct samples and evaluate feasibility of frequency measurements of poly(3-hexyl thiophene) (P3HT) thin films. 1Q 2006
- Complete measurements of the dielectric response of P3HT as a function of frequency and temperature. 3Q 2006

3. Integrated measurement platform: To directly compare OFET performance with its interfacial structure and chemistry, test structures have been fabricated on a single substrate that will include both active devices and pre-defined measurement regions. We will identify motifs that develop after processing and during operation that critically affect OFET performance. The use of an integrated substrate removes variations that may affect measurements performed separately. Specific test structures optimized to transfer information to industrial laboratories will be developed. We plan to provide electrical measurement protocols that will identify electronic signatures representative of performance-influencing structural changes and meaningful standard test methods.

DELIVERABLES:

- Measure field effect hole mobility, threshold voltage, and on/off ratios for P3HT OFETs spin-cast onto the test structure with varying spin-coating speeds. 4Q 2005

- Evaluate correlations between structural measurements and device performance of liquid crystalline polythiophene thin films. 4Q 2006.

Accomplishments

■ Near-edge X-ray absorption fine structure (NEXAFS) spectroscopy was applied to several classes of organic electronics materials to investigate the electronic structure, chemistry, and orientation of these molecules near a supporting substrate. In collaboration with the University of California-Berkeley, NEXAFS spectroscopy was used successfully to quantify the simultaneous chemical conversion, molecular ordering (Fig. 2), and defect formation of soluble oligothiophene precursor films for application in organic field effect transistors. Variations in field-effect hole mobility with thermal processing are directly correlated to the orientation and distribution of molecules within 3 nm to 20 nm thick films. Further, NEXAFS measurements on a series of oligothiophene precursors showed that the orientation development is strongly affected by the number of units in the core of the molecule and the change in the structure of the solubilizing group.

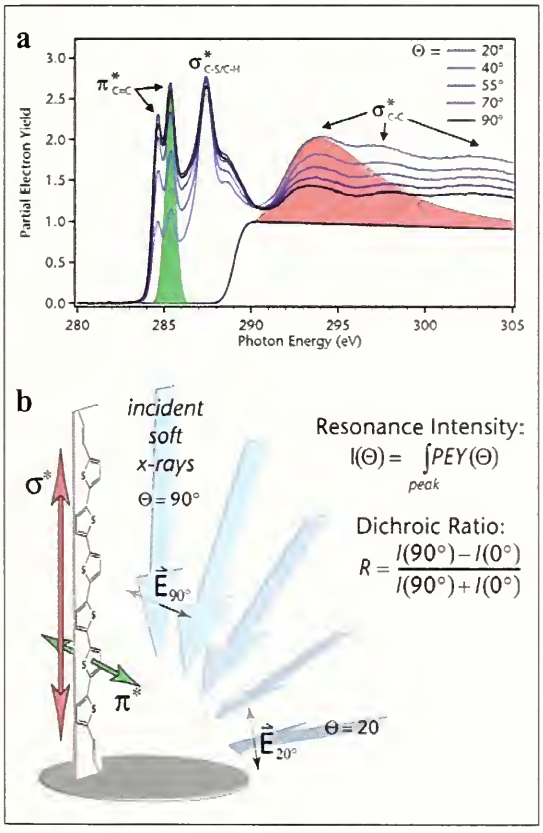

Figure 2. a, NEXAFS carbon K-edge spectra collected at changing incident angles from a film annealed at 200 °C. The green area indicates the oligothiophene π^* resonance used to determine planar orientation while the pink area indicates the σ^* resonance used to determine long axis orientation. b, Image depicting the orientation and spatial orientations of its primary K-edge carbon resonances. Blue arrows indicate incident polarized soft X-rays with electric field vectors extending normal to the plane of photon polarization.

■ A variety of polarized optical spectroscopies: infrared (IR) absorption, variable angle spectroscopic ellipsometry (SE), and near-edge X-ray absorption fine structure (NEXAFS) were applied in concert to investigate the structural evolution of poly(3-alkylthiophene) thin films induced by thermal processing. The combined spectroscopies determine the orientation distribution of the main chain axis (SE and IR), the conjugated π system normal (NEXAFS), and the side chain axis (IR). We find significant improvement in the backbone order of the films after heating above the melting point. Less aggressive thermal treatments are less effective. Interestingly, IR studies show that the changes in backbone structure occur without significant alteration of the structure of the alkyl side chains. The data indicate that the side chains exhibit significant disorder for all films regardless of annealing conditions.

■ Variations in the spin coating speed were used to systematically vary the solvent evaporation rate and the P3HT conjugated plane orientation was measured with NEXAFS spectroscopy. We find that the P3HT conjugated plane varies from an edge-on to a plane-on orientation as a function of the spin speed or solvent evaporation rate employed. This variation does not result in changes in surface morphology as observed by AFM, but it does correlate closely to the saturation hole mobility measured in field effect transistors. These results provide important insight into the structure formation in solution-processed conjugated molecules. Further, most additive patterning processes envisioned for solution-processable semiconductors will include a drying step, and the drying rate appears to be a critical variable in process design.

Collaborations

Polymers Division, MSEL – Jan Obrzut, C. K. Chiang, Brandon M. Vogel, Youngsuk Jung, R. Joseph Kline, Tatiana Psurek, Leah Lucas

Semiconductor Electronics Division, EEEL – Curt Richter, Oleg Kirillov, Eric Vogel

Ceramics Division, NIST – Daniel A. Fischer, Sharadha Sambasivan

Surface and Microanalysis Science Division, CSTL – Marc Gurau, Zachary Schultz

University of California, Berkeley – Amanda Murphy, Paul Chang, Jean Frechet, Vivek Subramanian

Stanford University – Mang-mang Ling, Zhenan Bao

Xerox – Liang Li, Beng Ong, Michael Chabinyc

Merck Chemicals – Iain McCulloch, Martin Heeney

Recent Publications

D. M. DeLongchamp, Y. Jung, D. A. Fischer, E. K. Lin, P. C. Chang, A. R. Murphy, J. M. J. Frechet, V. Subramanian, "Correlating Molecular Design to Microstructure in Thermally Convertible Oligothiophenes: The Effect of Branched vs. Linear End Groups." In press J. Phys. Chem. B (2006).

M. C. Gurau, D. M. DeLongchamp, B. M. Vogel, E. K. Lin, D. A. Fischer, S. Sambasivan, L. J. Richter, "Ordering in Poly(3-alkylthiophene) Thin Films Determined with Polarized Optical Spectroscopies," submitted to J. Chem. Phys. (2005).

M. L. Chabinyc, F. Endicott, B. D. Vogt, D. M. DeLongchamp, E. K. Lin, Y. Wu, B. S. Ong, "Effects of Humidity on Unencapsulated Poly(thiophene) Thin Film Transistors," (2005).

D. M. DeLongchamp, B. M. Vogel, Y. Jung, M. C. Gurau, C. A. Richter, O. Kirillov, J. Obrzut, D. A. Fischer, S. Sambasivan, L. J. Richter, E. K. Lin "Variations in semiconducting polymer microstructure and hole mobility with spin coating speed" Chem. Mater. 17, 5610 (2005).

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D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, P. Chang, A. R. Murphy, J. M. J. Fréchet, V. Subramanian, "Direct correlation of organic semiconductor film structure to field-effect mobility," Advanced Materials, 17, 2340 (2005).

J. Obrzut and K. Kano, "Impedance and Non-Linear Dielectric Testing at High A.C. Voltages Using Waveforms," IEEE Transactions on Instrumentation and Measurement (2005).

D. M. DeLongchamp, B. D. Vogt, C. M. Brooks, K. Kano, J. Obrzut, C. A. Richter, O. Kirillov, E. K. Lin, "Influence of a water rinse on the structure and electrical properties of poly(3,4-ethylene dioxythiophene):poly(styrene sulfonic acid) films," Langmuir 21, 11480 (2005).

J. Obrzut and A. Anopchenko, "Input Impedance of a Coaxial Line Terminated with a Complex Gap Capacitance - Numerical and Experimental Analysis" IEEE Transactions on Instrumentation and Measurement, **53**: 1197-1201 (2004).

Micro- and Nano-Electro-Mechanical Technology Metrology

Goal

The objective of this project is the development of test structures and test methodologies for the characterization of Micro-Electro-Mechanical and Nano-Electro-Mechanical Technology (MNT) fabrication processes. MNT is the extension of MEMS (Microelectromechanical Technology Systems) to include nanometer-scale technology. Full characterization of an MNT process requires accurate measurement of a large set of material properties, including Young's modulus, residual stress, thermal coefficients, surface roughness, density, and Poisson's ratio; dimensional metrology; and device parameters. Ideally these measurements should be quick, performed in the manufacturing line, with measurements at multiple locations across each wafer to allow characterization of process variation.

Customer Needs

Two NIST U.S. Measurement System (USMS) workshops have recently been held relating to MNT metrology.

The first USMS Workshop was held in Pittsburgh, PA on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions approximately seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" microelectromechanical systems (or MEMS). The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over $100 million) fabrication facility. This is similar to the foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop is in preparation and will be published in the MEMS Industry Group (MIG) 5-year anniversary report.

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, Florida. This meeting was targeted on metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

Technical Strategy

Overview: The MNT Metrology Project is currently championing MNT standardization efforts in two venues: ASTM and SEMI. Highlighting the need for MNT standardization is the number of companies and other organizations participating in these standards activities.

DELIVERABLES: MEMS Industry Group report, "Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies."

The first four MNT standards (on in-plane lengths, residual strain, strain gradient, and terminology) [1-4] originated in the ASTM E08.05.03 Task Group on Structural Films for MEMS and Electronic Applications. Also within this task group, standards for determining Young's modulus, ultimate strength, and fatigue for a surface micromachining process are being pursued via grants.

The MNT standardization efforts being actively pursued in SEMI's North American MEMS Standards Committee include recently-published SEMI Standard MS1-0306 on wafer-to-wafer bonding alignment targets. Other SEMI MNT standardization efforts include a proposed guide (PR9-0705) on microfluidic interfaces; a proposed standard (PR11-1105) on MEMS terminology; and work on stiction, wafer specifications, wafer bond inspection techniques, wafer bond strength, and RF MEMS qualification.

An additional activity in SEMI's MNT standardization effort is the identification of standards related to MNT technology. SEMI is attempting to identify these standards and incorporate them into SEMI's "Living Standard." This Living Standard, which will list MNT standards from all standardization bodies and be maintained by the N.A. MEMS Standards Committee, will serve to guide industry and researchers to existing standards and highlight areas where standards may be needed.

DELIVERABLES: Draft "Living Standard," and easy-to-access SEMI Standards Web page incorporating, for example, a compilation of all MNT standards and pertinent links for purchasing. 3Q 2006

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C. McGray
R. Allen

Finally, the MNT Metrology project has undertaken development of dimensional metrology test structures and techniques for microfluidics applications. The goal of this work is standard test structures, methods, and analysis techniques such as exist for semiconductor devices.

NIST's role: Activities of the MNT Metrology Project include the following:

1. Keeping tabs on the progress of the various standardization efforts via attending standardization meetings (such as ASTM and SEMI) and maintaining the "Living Standard" for SEMI's N.A. MEMS Standards Committee.

2. Facilitating a collaborative research process between the different parties and acting as a neutral intermediary in shepherding the measurement techniques through the standardization process, if necessary.

3. Providing technical assistance to others during the standardization effort, if necessary (and given the appropriate resources).

4. Although the completion of each standard will have its own "character," given NIST's experience with the completion of the four ASTM MEMS standards, guidance can be provided as to what is involved in the completion of a standard test method and lessons learned along the way.

5. Narrow in on the next material properties to work on at NIST and follow through with the work, if appropriate. Currently, the next parameters being considered for standardization are thickness, Young's modulus, residual stress, and residual stress gradient as described below:

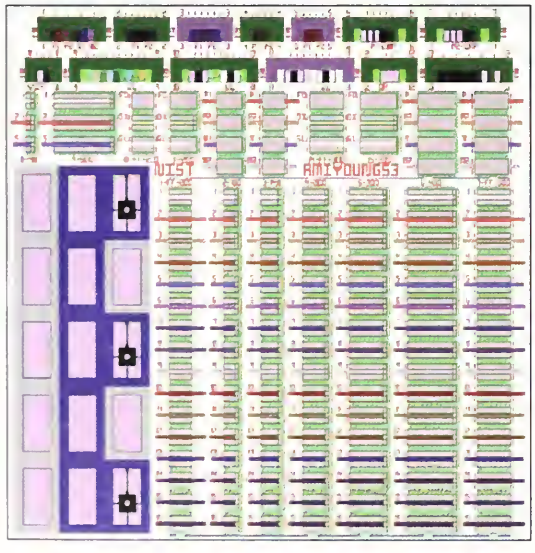

Figure 1. CMOS test chip design incorporating thickness test structures, cantilevers, fixed-fixed beams, and tensile test structures.

Thickness: To measure the 35 thicknesses for the 48 *p*-well, CMP designs over field oxide and over *n*-doped active area for a 1.5 µm commercial CMOS process, an electro-physical technique is used which combines a physical approach and an electrical approach. The physical approach obtains thicknesses from step height measurements on thickness test structures using a non-contact optical interferometer. (Figure 1 shows a test chip design with thickness test structures along the top edge of the chip. A design rendition of a sample thickness test structure is given in Fig. 2a, with its cross-section given in Fig. 2b.) The electrical approach obtains thicknesses from MOSIS-supplied capacitances, MOSIS-supplied sheet resistances and MOSIS-supplied resistivities, crystalline lattice calculations, and the equating of similar oxides between platforms. The thickness from the approach that results in the lowest value for the combined standard uncertainty, u_c, is the reported value.

For standardization, the above method will require simplification in order to apply to more than one process.

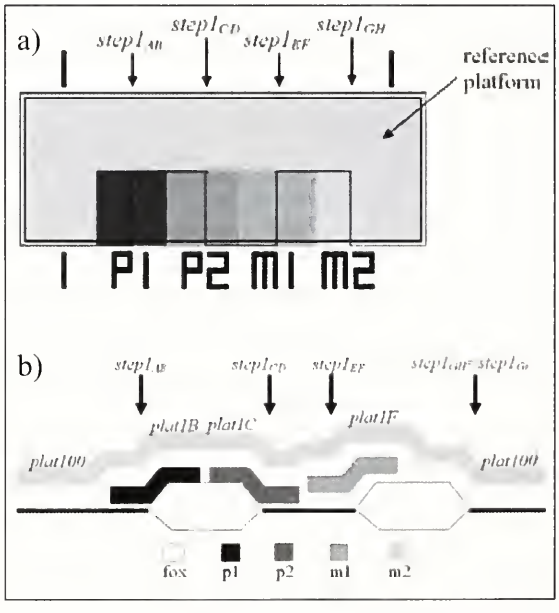

Figure 2. For a thickness test structure: a) a design rendition and b) a cross-section.

Young's modulus: The resonant frequencies of 16 independently designed CMOS cantilevers as measured with an optical vibrometer are used to find the Young's modulus values of the various layers in the process. These frequencies in addition to the thicknesses as obtained using the electro-physical technique described above are the inputs to an optimization program, which outputs the Young's modulus values.

ASTM E 2244–05, "Standard Test Method for In-Plane Length Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

ASTM E 2245–05, "Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

ASTM E 2246–05, "Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

J. C. Marshall, E. M. Secula, and J. Huang, "Round Robin for Standardization of MEMS Length and Strain Measurements," SEMI Technical Symposium: Innovations in Semiconductor Manufacturing (STS: ISM), SEMICON West 2004, San Francisco, CA, July 12-14, 2004.

J. C. Marshall, "MEMS Length and Strain Measurements Using an Optical Interferometer," NISTIR 6779, August 2001.

MEMS Length and Strain Calculator Web site: http://www.eeel.nist.gov/812/test-structures/MEMSCalculator.htm.

For standardization, the above method will require simplification in order to apply to more than one process. It is envisioned that this method will be beneficial to the nano-world when studying such things as nanoscale cantilever-based physical, chemical, and biological sensors.

Residual stress and its gradient: As an extension of the above mentioned thickness and Young's modulus work, CMOS cantilevers and fixed-fixed beams can be fabricated on the same chip (as given in Fig. 1). The cantilevers can be used to find the strain gradient and Young's modulus values and the fixed-fixed beams can be used to find residual strain. Given these measurements, the residual stress and its gradient can be calculated. High values of residual stress lead to failure mechanisms in ICs such as electromigration, stress migration, and delamination. Knowledge of the residual stress values can be used to improve the yield in CMOS fabrication processes.

DELIVERABLES: The results of our work will be presented at the appropriate standards organization and in articles for publication. 1Q 2007

Accomplishments

■ *Thickness:* The electro-physical technique proved successful in finding the thicknesses of all the layers in the 1.5 μm commercial CMOS foundry process with relatively low values for u_c (between 0.00012 μm and 0.056 μm for a given processing run). In addition, an earlier version of this technique has been verified via the successful optimization of the Young's modulus values for the various layers in the process.

A virtual transition region was found between the physical and the electrical approach, which is based upon the value of u_c. For the presented data set, the transition region is between the u_c values of 0.0073 μm and 0.013 μm, where the electrical approach tended to be used for the smaller values of u_c (which can be viewed as those layers which tend to be fabricated earlier in the processing sequence) and the physical approach used for the larger values of u_c.

The electro-physical technique is detailed in a 30-page paper, which is currently being reviewed.

■ *Young's modulus:* The test chip design given in Fig. 1 includes cantilevers ranging in length from 100 μm to 400 μm. (A procedure was developed using the optical vibrometer to obtain the resonant frequencies of the shorter length cantilevers.) Plots of Young's modulus versus length for each layer exhibit phenomenal results. *The optimized Young's modulus results are stable as a function of length and within the realm of acceptability!* Figure 3 shows these plots for metal1 and metal2. The data points given at L=500 μm represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by '*Eguess*' is the initial value used in the optimization. An initial result from tensile tests done by David Read at NIST-Boulder found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal2 lines in Fig. 3.

The resonant frequency technique for finding the Young's modulus values is presented in an article prepared for Electron Device Letters, which is currently being reviewed by a co-author.

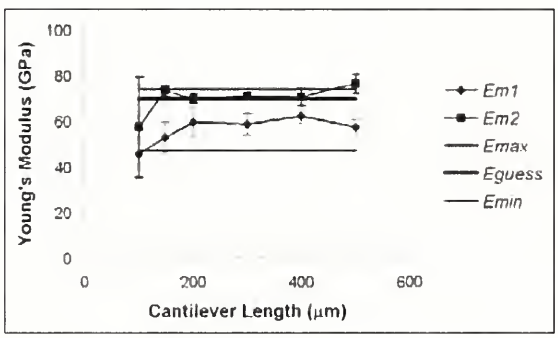

Figure 3. Optimized Young's modulus values for metal1 and metal2 versus length.

Collaborations

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Veriner.

Klaros Corporation, Beallsville, MD Robert I. Scace.

BayTech Group, 30 Winsor Way, Weston, MA, Winthrop A. Baylies.

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read.

Others (current and/or future): Coventor, Inc., Pennsylvania State Univ., Fraunhofer Inst. (Germany), MEMSCAP, Sandia, and others not yet identified.

Recent Publications

ASTM E 2444–05$^{\varepsilon 1}$, "Standard Terminology Relating to Measurements Taken on Thin, Reflecting Films," January 2006.

J. C. Marshall, R. I. Scace, and W. A. Baylies, "MEMS Length and Strain Round Robin Results with Uncertainty Analysis," NISTIR 7291, January 2006.

NIST's Center for Nanoscale Science and Technology Nanofab

Technical Contacts:
R. Celotta
G. Henein

Goals

The NIST Center for Nanoscale Science and Technology (CNST) Nanofab will:

- Enable fabrication of prototypical nanoscale test structures, measurement instruments, standard reference materials, electronic devices, magnetic devices, MEMS, and bio-devices critical to NIST's Strategic Focus Areas (Nanotechnology, Homeland Security, Healthcare) and the nation's Nanotechnology Needs
- Provide access to expensive nanofabrication tools, technologies and expertise in a shared-access, shared-cost environment to NIST and its partners
- Foster internal collaboration in Nanotechnology across NIST's Laboratories
- Foster external collaboration in Nanotechnology with NIST's partners.

Customer Needs

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in the face of heightened global competition, NIST has constructed one of the most technologically advanced facilities in the world — the Advanced Measurement Laboratory, or AML. The CNST Nanofab (Fig. 1) is one of five buildings in the AML at the Gaithersburg, MD campus. The Nanofab provides researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices.

Figure 1. Main entrance to the AML showing the CNST Nanofab on the left.

Technical Strategy

The AML contains two above ground instrument buildings, two completely below ground metrology buildings, and one Class 100 clean room building housing the CNST Nanofab. The AML provides NIST with superior vibration, temperature and humidity control, and air cleanliness. The CNST Nanofab has approximately 1000 m^2 of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wafers) that is now fully operational (Fig. 2). This includes wet chemical wafer cleaning stations, furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, four reactive ion etchers (SF_6/O_2, Fl Metal, Cl Metal, Deep), one XeF_2 isotropic silicon etcher, five metal deposition tools (three thermal, one e-beam, one sputterer), contact lithography (front- and back-side alignment), nanoimprint lithography, converted SEM e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, etc.). A state-of-the-art e-beam lithography system with mask making capability is scheduled for installation during the Fall of 2006.

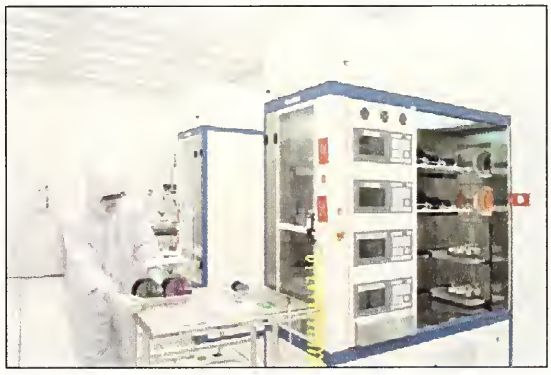

Figure 2. Oxidation and annealing furnaces banks.

The Nanofab is operated as a shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, are permitted to independently operate the equipment. The tools are operated in a manner such that a wide variety of materials can be processed. The facility is part of NIST's Center for Nanoscale Science and Technology. Unlike other nanofabs, the NIST nanofab is unique in that it is

located next to the most advanced metrology tools in the world (AML), and its focus is the fabrication of nanoscale structures necessary for metrology and standards in support of the semiconductor industry, nanotechnology, biotechnology, and homeland security.

DELIVERABLES: E-beam lithography system fully operational. 4Q 2006

Metrology for Spintronic Devices

Technical Contacts:
J. Unguris
R. Goldfarb

"Imaging and metrology of magnetic structures are at the heart of the systematic development and characterization of magnetoelectronic materials and devices"

WTEC Panel on SPIN ELECTRONICS Final Report August 2003 (p.18).

Goals

The overall goal of the Metrology for Spintronic Devices program is to develop the metrological tools that will enable the development of electronic devices that exploit the electron spin degree of freedom in addition to its charge. Present spintronic devices include magnetic random access memory (MRAM), which has the possibility of becoming a "universal" memory element, hard-disk drive read heads, and other highly-compact magnetic memory devices, such as those based on current induced domain-wall motion in magnetic wires. In addition, spintronic devices also present an avenue towards replacing conventional complementary metal oxide semiconductor (CMOS) technology as device dimensions shrink into the deep nanometer regime, development of entirely new device structures such as nanoscale microwave components for on-chip spectral analysis, nanoscale timing elements, and microwireless communication architectures. In each case, a fundamental understanding of the interactions between a spin-polarized current and ferromagnetic metals and semiconductors is a necessity. The particular goal of this project is to develop the metrology and perform the fundamental measurements to enable the development of these spin-based devices.

An additional goal is to enable the development of magnetoelectronic and spintronic devices by using Scanning Electron Microscopy with Polarization Analysis (SEMPA) to directly image the nanoscale magnetic structure and correlate the magnetic structure with device performance.

Customer Needs

MRAM elements are currently being shipped to customers for incorporation into products which are expected to be commercially available by the end of 2006. The magnetic memory elements are expected to enter the marketplace at the 180 nm lithography node. Although no public roadmap for MRAM exists, companies such as IBM and Freescale Semiconductor expect that the present circuit architecture, which relies on switching (writing) using applied magnetic fields, will not be viable beyond the 65 nm lithography node. These limitations arise because the scaling laws associated with the stability of the magnetic structures used in MRAM devices: As the device dimensions are decreased, the magnetic elements are required to have increased stability against thermal fluctuations. This, in turn, will require larger writing fields, which cannot be supported in the present device architecture. It is expected that a new switching mechanism will be required for scaling MRAM devices below the 65 nm node. One way to circumvent this scaling limitation is to switch the elements through the use of spin-polarized currents flowing *through* the memory elements to switch (write) them via the spin transfer effect. While this switching mechanism is largely expected to allow continued scaling of MRAM elements, it has been experimentally demonstrated only within the last five years, and the present understanding of the effect remains only qualitative. In order to enable the continued scaling of MRAM devices, the fundamental metrology and measurement of the intrinsic scaling laws associated with the spin transfer effect are a necessity. In particular, methods to definitively relate threshold switching currents to fundamental materials properties need to be developed, materials damping parameters need to be measured as a function of device size, and tunnel junction characteristics need to be understood at the atomic scale.

The performance, and ultimately the commercial viability, of magnetoelectronic devices such as Magnetic Random Access Memories (MRAM) or magnetic field sensors depend on understanding and controlling their magnetic nanostructure. Nanoscale magnetic features such as domains, domain walls, anisotropy dispersion, edge effects, grain structure, and defects critically affect device performance. Imaging these magnetic nanostructures requires techniques with high spatial resolution and high magnetic sensitivity that do not disturb the tiny amount of magnetic material used in a device. SEMPA has 10 nm spatial resolution, 1000 Fe atom sensitivity, and is nondestructive while imaging. Furthermore, SEMPA images the magnetization directly allowing direct comparisons with computer generated micromagnetics simulations of ideal devices.

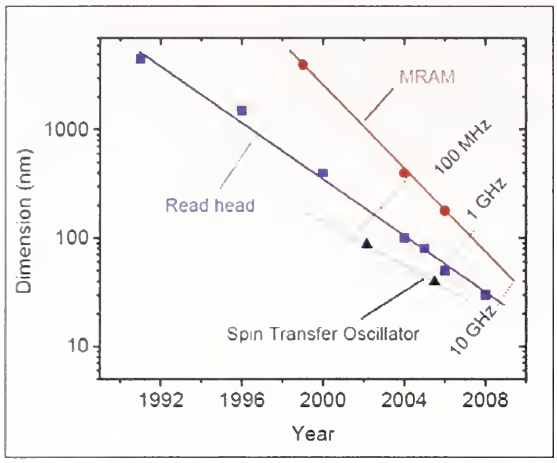

Figure 1. Within a few years, critical device dimensions will be less than 100 nm. Magnetic field based switching of MRAM is no longer feasible at the 65 nm node and alternative switching mechanisms will required. Similar scalability limitations are also expected in CMOS devices. Source: NIST Electromagnetics Division.

More generally, many semiconductor devices encounter scaling limitations as the device dimensions shrink into the deep nanometer regime. For instance, present CMOS scaling laws indicate that the devices will encounter both quantum mechanical and fabrication limitations below the 10 nm length-scale. One potential avenue towards circumventing this roadblock is spin-based devices, which afford the possibility of fast operation, low power-dissipation, and general compatibility with CMOS-based device fabrication. Furthermore, novel effects which occur only at the nanoscale in hybrid ferromagnetic systems can also be exploited to provide new functionality in nanoscale devices. These devices point a way to creating new nanoscale systems such as on-chip spectral analysis, nanoscale microwave generators, as well as nanoscale microwave mixers, phase discriminators, and chip-to-chip wireless communication schemes. However, as with the spin-based memory devices, in order for these spin-enable devices to be commercially realized, the fundamental measurement techniques required to understand the interactions between spin polarized electrons and ferromagnetic materials need to be developed and implemented.

Technical Strategy

The technical strategy is to develop the metrology and perform the fundamental measurements to characterize and understand the effects of spin-polarized currents in spin-based magnetic nanostructures. Particular attention will be paid to the intrinsic scaling laws associated with device switching times in both all-metallic and magnetic tunnel junction MRAM structures, as well as the thermal contributions to the critical current densities. These measurements will help to provide a basis for scaling of MRAM devices below the 65 nm node and provide a basis for evaluating the potential of nanoscale spintronic devices for replacing/augmenting CMOS in the deep nanometer regime.

1. Develop method to determine intrinsic current-based switching threshold in all metallic MRAM structures.

DELIVERABLES:

- Characterize thermally activated current induced switching in all-metallic MRAM structures. Complete measurements in 4Q 2005.
- Measure high speed switching in all-metallic devices ranging from 50 nm to 150 nm and extrapolate the value of the intrinsic switching threshold. Compare extrapolated value to the value measured at low temperature. Complete measurements in 2Q 2006 and submit paper.

2. Determine scaling of magnetic damping parameter with device size.

DELIVERABLES: Measure damping parameter in a variety of magnetic nanostructures with dimensions between 100 nm and 1 micrometer and compare those measurements of damping in continuous films. Complete measurements in 2Q 2006 and submit paper.

3. Characterize noise and current induced switching tunnel junction based MRAM devices.

DELIVERABLES:

- Measure and characterize low frequency noise in high-quality aluminum oxide based magnetic tunnel junctions. Complete measurements in 3Q 2006 and submit paper.
- Measure threshold for current induced switching in tunnel junction based MRAM devices at below 1 ns for device sizes ranging from 50 nm to 150 nm. Compare results with those obtained from all-metallic based structures and theoretical models. Complete measurements in 4Q 2006 and submit paper.

Although SEMPA is already an established tool for imaging magnetic nanostructures in simple ferromagnetic structures, special protocols and instrumentation need to be developed for imaging the magnetization in samples that are operationally as close as possible to commercial magnetoelectronic devices. In particular, sample preparation techniques that expose the ferromagnetic

element directly to the SEMPA probe need to be developed. Of course these cleaning procedures, which will involve techniques such as ion milling, must not disturb the magnetic structure under investigation. Second, since a critical question is the behavior of magnetic nanostructures in a functioning device, instrumentation will be developed to allow magnetic imaging while the device is electrically active *i.e.*, while applying magnetic fields or measuring magnetoresistance.

1. Image simple static devices that are the same size and shape as real devices, but are not electrically active or covered with capping layers.

DELIVERABLES: SEMPA images of magnetic nanostructure in patterned devices made from bare ferromagnetic films and multilayers. 2Q 2006

2. Develop cleaning procedures to expose magnetic material in more complex, multilayer device structures where the magnetic structures are buried under nonmagnetic layers. Determine *in-situ* ion milling protocols that can remove nonmagnetic coatings without disturbing the magnetization.

DELIVERABLES: SEMPA images of buried magnetic nanostuctures. 3Q 2006

3. Construct custom sample holders to enable magnetic imaging of electrically active magnetoelectronic devices. These sample holders will allow up to seven different electrical connections per sample without compromising the electron microscope's load lock or goniometer operation.

DELIVERABLES: SEMPA images of devices while applying magnetic fields and measuring magnetoresistance. 4Q 2006

Accomplishments

■ *High-speed Current Induced Switching for MRAM Devices:* In collaboration with Hitachi Global Storage Technologies (HGST) and Freescale Semiconductors we have demonstrated sub-nanosecond (290 ps) switching of nanoscale MRAM devices is possible via the spin transfer effect. To date this is the shortest switching time that has been reported in the literature. The inverse switching time (*i.e.*, the switching frequency) at room temperature is linearly proportional to the current applied to the device. This finding is in accordance with the behavior expected from theoretical considerations and indicates that the measured room-temperature switching threshold is strongly affected by thermal fluctuations in the nanoscale devices. By extrapolating the measured switching current to zero applied pulse width, the *theoretical* value of the intrinsic device critical current can be determined. However, this theoretical method of determining the intrinsic switching thresholds (*i.e.*, those related to materials properties and device size) from stochastic, thermally activated switching events had not been experimentally verified. By extensively comparing the thresholds for current driven switching at room temperature and 4 K for a range of applied field values, we have been able to verify the extrapolation methods used to infer the intrinsic switching current, identify thermal contributions to the switching threshold, and determine the materials/device parameters that are responsible for setting the intrinsic switching threshold. These measurements will allow for improved device design and reliability for future MRAM at the 65 nm node and beyond.

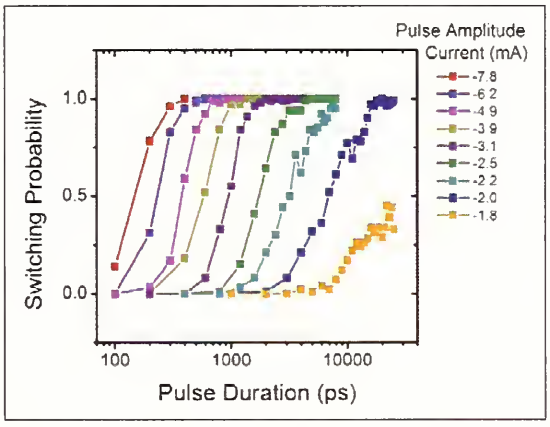

Figure 2. High speed current induced switching of all-metallic MRAM structures. The data show that the switching frequency is roughly linearly proportional to the threshold switching current. Source: S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, J. A. Katine, and M. Carey, Spin transfer switching of spin valve nanopillars using nanosecond pulsed currents, Journal of Magnetism and Magnetic Materials 286, 375-380 (2005).

■ *Damping in Magnetic Nanostructures:* One of the critical parameters in determining the threshold switching current in magnetic devices is the magnetic damping parameter; the larger the damping in the system, the larger the current required to switch the device. While the material dependent damping parameters have been routinely measured in macro/microscopic devices, very little is known about how damping is affected when device sizes are decreased to the

nanometer length scale. As device dimensions are decreased, the surfaces of devices become increasingly important. This is particularly the case for damping in magnetic nanostructures. Nanomagnetic devices will typically have oxidation of the ferromagnetic materials on at least some of their sides, and ferromagnetic oxides are well known sources of damping. Recently some researchers have shown *indirect* evidence that the magnetic damping in magnetic nanostructures can be increased by more than a factor of ten relative to that of macroscopic devices. We have recently developed the metrology capabilities to *directly* measure the magnetic damping in a variety of magnetic systems over a wide range of device sizes. While the measurements will be limited to giving the average properties of device arrays, we expect that the information we gain will yield significant insights into the hierarchy of damping mechanisms in magnetic nanostructures. Measurements are presently underway. We are also exploring new measurement methods which will allow accurate damping measurements of individual magnetic nanostructures.

■ *Noise and Current Induced Switching in Magnetic Tunnel Junction Devices:* Currently, typical spin transfer based MRAM structures are based on all-metallic structures. These structures have resistances on the order of 5–10 ohms and are poorly impedance matched to standard semiconductor circuitry. While this impedance mismatch will become less severe as device dimensions are decreased, it will likely be necessary to implement magnetic tunnel junction (MTJ) devices. However, in general, there is also an increase in noise, particularly at low frequency, when incorporating tunnel junctions into device structures, which can degrade device performance and read-out fidelity. The low-frequency noise is associated with defects and atomic scale variations in the barrier. We have successfully measured and characterized this excess noise in high-quality aluminum oxide magnetic tunnel junctions with dimensions on the order of several micrometers and used Lorentz transmission electron microscopy (TEM) imaging to investigate the correlation between electronic noise and the structural properties of the barrier. Work is presently underway to incorporate these tunnel junction barriers into nanometer scale MRAM devices in order to investigate both current induced switching and noise in nanoscale MTJ devices.

We have systematically measured the magnetic structure of prototypical magnetic sensor elements as a function of size. The large magnification range of SEMPA enables imaging devices that vary from millimeter to nanometer dimensions. This work quantitatively demonstrated the transition from shape dominated, to exchange dominated magnetic structure as the size of these structures was reduced (Fig. 3).

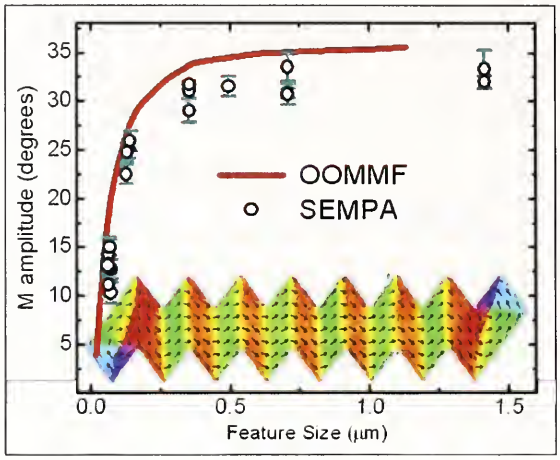

Figure 3. SEMPA image of a magnetic sensor element, and a plot of the amplitude of magnetic fluctuations versus device size. As the device gets smaller, exchange interactions prevent the magnetization from following the shape of the device and the amplitude decreases in agreement with micromagnetic (OOMMF) simulations.

We have successfully imaged MRAM prototypes provided by IBM (Fig. 4, page 189). These patterned structures consist of bare ferromagnetic films grown on antiferromagnetic films. Instead of the magnetization being simply aligned either along or opposite to the element axis, SEMPA images show considerable fluctuation of the magnetization direction within an element. The anisotropy dispersion is possibly due to the polycrystalline nature of the anitferromagnetic film used for exchange biasing, and can lead to problematic variations of the magnetic switching field for these devices.

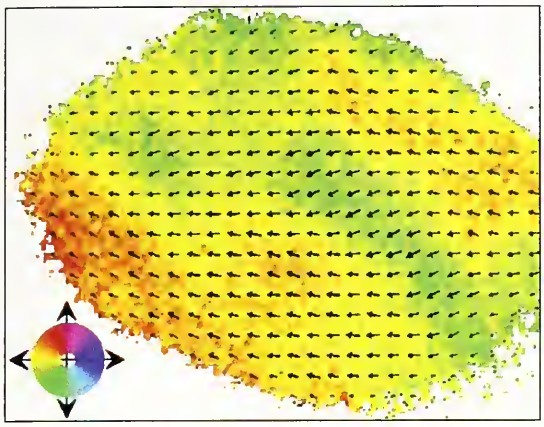

Figure 4. SEMPA image of an 0.5 μm MRAM element. Although the element is nominally magnetized in one direction, variations of the magnetization direction within the element are seen both in the variations in color (related to magnetization direction by the colorwheel) and by the overlaid arrow field.

We have imaged spin torque induced domain wall motion in nanoscale wires. The spin torque associated with the high current density in a ferromagnetic nanostucture can be used to switch the magnetic state or to move magnetic domain walls. Being able to manipulate the state of a magnetic device without applying a magnetic field is appealing for high density magnetic memory applications. We have prepared magnetic wires with different dimensions and investigated how the spin polarized current affects domain walls in these wires. SEMPA images reveal that the spin torques not only push the domain walls along the wire, but can also distort the walls, and, in some cases, convert the domain walls from one type to another (see Fig. 5).

Collaborations

IBM, MRAM device imaging and thermal induced noise in tunnel-junction based MRAM devices.

Freescale Semiconductor, MRAM device imaging and incorporating magnetic tunnel junctions into MRAM devices.

Hitachi Global Storage Technologies, high-speed switching in all-metallic MRAM devices.

Seagate Technologies, phase-locking mechanisms in spintronic microwave oscillator arrays.

Cornell University, damping in ferromagnetic systems.

U.S. Army Research Laboratory, imaging magnetic sensors

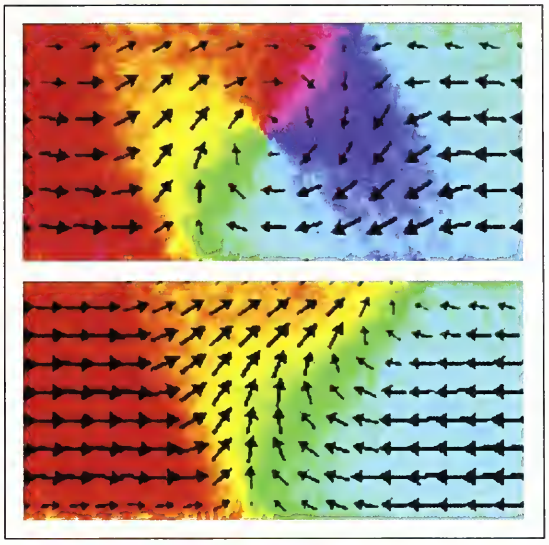

Figure 5. SEMPA images of current induced domain wall transitions in a 300 nm wide ferromagnetic wire. The spin torque associated with the current moves the domain walls along the wires, but it also causes the walls to switch from vortex to transverse wall structures.

Future Opportunities

Nanoscale spintronic devices also provide an opportunity for the development of dense non-volatile memory elements as well as new spin-enabled nanoscale microwave devices, such as microwave sources and mixers for timing, communications, and spectral analysis applications. In addition, they also provide one potential avenue towards replacing/augmenting conventional CMOS devices in the deep nanometer regime. As such, we expect that spintronic devices hold the potential to have a great impact on the semiconductor industry, particularly as device dimensions shrink into the nanoscale. The goal of this project is to provide the fundamental metrology and measurements to enable the development of this wide range of devices and applications.

Recent Publications

W. C. Uhlig and J. Unguris, *"Size Dependent Transition from Shape to Exchange Dominated Magnetic Nanostructures in Patterned Zigzags,"* Journal of Applied Physics **99**, 08G302 (2006).

S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, and J. A. Katine, *"Mutual phase-locking of microwave spin torque nano-oscillators,"* Nature **437**, 389-392 (2005).

W. H. Rippard, M. R. Pufall, S. Kaka, T. J. Silva, S. E. Russek, and J. A. Katine, *"Injection locking and phase control of spin transfer nano-oscillators,"* Physical Review Letters **95**, 067203 (2005).

S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, J. A. Katine, and M. Carey, *"Spin transfer switching of spin valve nanopillars using nanosecond pulsed currents,"* Journal of Magnetism and Magnetic Materials **286**, 375-380 (2005).

S. E. Russek, S. Kaka, W. H. Rippard, M. R. Pufall, T. J. Silva, and M. Donahue, *"Micromagnetic modeling of nano-contact spin-transfer oscillators,"* San Jose, Magnetism and Magnetic Materials Conference, ES-25, 2005.

S. E. Russek, S. Kaka, W. H. Rippard, M. R. Pufall, and T. J. Silva, *"Finite-temperature modeling of nanoscale spin-transfer oscillators,"* Physical Review B **71**, 104425 (2005).

M. R. Pufall, W. H. Rippard, S. Kaka, T. J. Silva, and S. E. Russek, *"Frequency modulation of spin-transfer oscillators,"* Applied Physics Letters **86**, 082506 (2005).

W. H. Rippard, M. R. Pufall, S. Kaka, T. J. Silva, and S. E. Russek, *"Direct-current induced dynamics in $Co_{90}Fe_{10}$/$Ni_{80}Fe_{20}$ point contacts,"* Physical Review Letters **92**, 027201 (2004).

F. C. S. da Silva, W. C. Uhlig, A. B. Kos, S. Schima, J. Aumentado, J. Unguris, and D. P. Pappas, *"Zigzag Shaped Magnetic Sensors,"* Applied Physics Letters **85**, 6022 (2004).

C. A. F. Vaz, L. Lopez-Diaz, M. Kläui, J. A. C. Bland, T. L. Monchesky, J. Unguris, and Z. Cui, *"Observation of a Geometrically Constrained Domain Wall in Epitaxial FCC Co Small Disks,"* Journal of Magnetism and Magnetic Materials **272-276**(3), 1674-1675 (2004).

C. A. F. Vaz, T. L. Monchesky, J. Unguris, E. Bauer, S. Cherifi, S. Heun, A. Locatelli, L. J. Heyderman, Z. Cui, and J. A. C. Bland, *"Spin Configurations and Classification of Switching Processes in Mesoscopic Ferromagnetic Rings Down to Sub-100 nm Dimensions,"* Journal of Magnetism and Magnetic Materials **272-276**(3), 1631-1636 (2004).

BioElectronics Metrology

Goals

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study neural single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Customer Needs

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nano-fabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

Technical Strategy

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in-vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in-vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We are focusing our initial research efforts on the study of retinal (neuronal) cells and will later progress to other cell systems.

DELIVERABLES:

- Develop an array of micro-electrochemical cells and methods to pattern cells on the array for single-cell electrochemical measurements. 3Q 2007

Technical Contacts:
M. Gaitan
J. J. Kasianowicz
D. R. Reyes
B. J. Polk

- Microfluidic and microelectronic components on a single platform for delivering precise chemical stimuli to single cells. 1Q 2007
- Characterization of the single-cell culture response to glutamate with PEDF as a neurotrophic factor. 3Q 2007
- Develop integrated rf/microwave structures for controlling the temperature of single-cell culture chambers and/or for manipulating cells. 4Q 2006
- Continuous monitoring of cell growth, development and viability in the presence and absence of therapeutic drugs and chemical toxins. 3Q 2007

Accomplishments

■ We developed a method to adhere retinal cells on micropatterned polyelectrolyte multilayer (PEM) lines adsorbed on poly(dimethylsiloxane) (PDMS) surfaces using microfluidic networks. PEMs were patterned on flat, oxidized PDMS surfaces by sequentially flowing polyions through a microchannel network that was placed in contact with the PDMS surface. Polyethyleneimine (PEI) and poly(allylamine hydrochloride) (PAH) were the polyions used as the top layer cellular adhesion material. The microfluidic network was lifted off after the patterning was completed and retinal cells were seeded on the PEM/PDMS surfaces. The traditional practice of using blocking agents to prevent the adhesion of cells on unpatterned areas was avoided by allowing the PDMS surface to return to its uncharged state after the patterning was completed. The adhesion of rat retinal cells on the patterned PEMs was observed five hours after seeding. Cell viability and morphology on the patterned PEMs were assayed. These materials proved to be nontoxic to the cells used in this study regardless of the number of stacked PEM layers. Phalloidin staining of the cytoskeleton revealed no apparent morphological differences in retinal cells compared with those plated on polystyrene or the larger regions of PEI and PAH (Fig. 1, left panel); however, cells were relatively more elongated when cultured on the PEM lines. Cell-to-cell communication between cells on adjacent PEM lines was observed as interconnecting tubes containing actin that were a few hundred nanometers in diameter and up to 55 mm in length (Fig. 1, center panel). This approach provides a simple, fast, and inexpensive method of patterning cells onto micrometer-scale features.

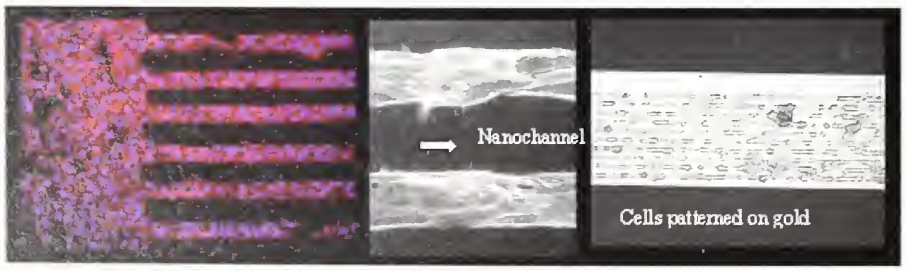

Figure 1. The left and center panels are images of R28 cells retinal patterned using polyelectrolyte multilayers lines adsorbed on poly(dimethylsiloxane). The center panel shows a nanochannel that was spontaneously formed by the cells. The right panel is an image of cells patterned on a gold surface using the polyelectrolyte multilayers.

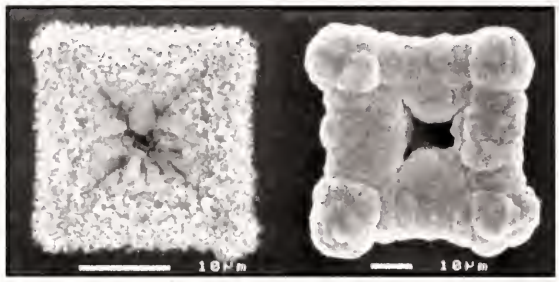

Figure 2. SEM images of two silver nanopores formed by electroplating on micromachined silicon micropores.

■ We developed a method to create nanofluidic restrictions by electroplating silver on micrometer scale pores. Electrodeposition of silver was investigated as a fabrication tool for constricting large (10^3 μm^2) vias in silicon substrates while leaving a small opening in the center of the via. Silver reduction from ammoniacal silver nitrate was studied at electrodes of novel geometry (*i.e.*, the edge of the vias) with respect to reduction potential, reduction pulse type, and pulse duration. A variety of crystal nucleation and growth patterns was observed and characterized by scanning electron microscopy (Fig. 2). It was found that electroplated silver occluded the vias to leave open areas of less than 1 μm^2. Such occlusions might be used as restrictions in microfluidics systems, forming a type of solid-state micropore or nanopore.

■ A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with miniaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by electroplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes (Fig. 3, left panel). The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microrefer-

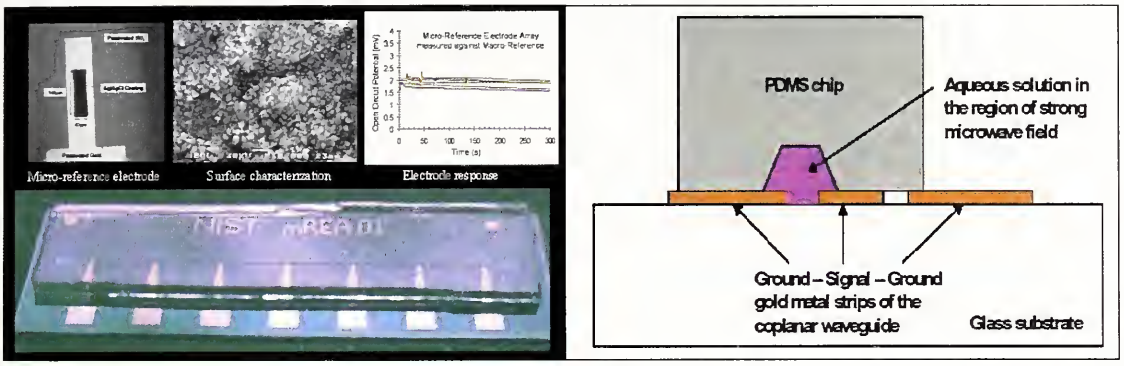
Micro-reference electrode
Surface characterization
Electrode response
PDMS chip
Aqueous solution in the region of strong microwave field
Ground – Signal – Ground gold metal strips of the coplanar waveguide
Glass substrate

Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

ence electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

■ Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (μTAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). A new approach for temperature cycling of microfluidic systems is presented that is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel (Fig. 3, right panel). We demonstrate that the microwave signal can be tuned to most effectively deliver the heat to the fluid at a frequency of 18 GHz (in agreement with theory) independent of the ionic strength of the solution. This approach will have application to microwave assisted chemistries which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. This paper suggests that those advantages can also be realized in a microfuidic format.

■ We have integrated electrodes within microfluidic devices to carry out a.c. dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using a.c. dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

Recent Publications

S. P. Forry, D. R. Reyes, M. Gaitan and L. E. Locascio *"Facilitating the Culture of Mammalian Nerve Cells with Polyelectrolyte Multilayers,"* Langmuir, in press.

B. J. Polk, A. Stelzenmuller, G. Mijares, W. MacCrehan, and M. Gaitan, *"Ag/AgCl Microelectrodes with Improved Stability for Microfluidics,"* Sensors and Actuators B, 114: 239-247, 2006.

B. Nablo, K. M. Halverson, R. G. Panchal, S. Bavari, T. L. Nguyen, R. Gussio, M. Misakian and J. J. Kasianowicz, *"Biophysical properties of the Bacillus anthracis PA63 ion channel,"* Biophysical Journal 90 (1): B179-B179 Suppl. S, (2006).

S. P. Forry, D. R. Reyes, B. J. Polk, M. Gaitan and L. E. Locascio, *"Generating Cell Arrays in Microfluidic Networks,"* Proc. MicroTAS 2005 Conference, Boston, MA, pp. 1398-1400, 2005.

S. Sundaresan1, B. J. Polk, D. R. Reyes, V. R. Mulpuri and M. Gaitan, *"Temperature Control of Microfluidic Systems by Microwave Heating,"* Proc. MicroTAS 2005 Conference, Boston, MA, pp. 657-659, 2005.

D. K. Shenoy, W. R. Barger, A. Singh, R. G. Panchal, M. Misakian, V. M. Stanford, and J. J. Kasianowicz, *"Functional reconstitution of protein ion channels into polymerizable phospholipid membranes,"* Biophysical Journal 88 (1): 552A-552A Part 2 Suppl. S, 2005.

K. M. Halverson, R. G. Panchal, T. L. Nguyen, R. Gussio, S. F. Little, M. Misakian, S. Bavari, and J. J. Kasianowicz, *"Electrophysiological analysis of anthrax toxin interactions,"* Biophysical Journal 88 (1): 476A-477A Part 2 Suppl. S, 2005.

J. J. Kasianowicz, *"Nanopores - Flossing with DNA,"* Nature Materials 3 (6): 355-356 JUN 2004.

B. J. Polk, M. Bernard, J. J. Kasianowicz, M. Misakian, and M. Gaitan, *"Microelectroplating silver on sharp edges toward the fabrication of solid-state nanopores,"* Journal of the Electrochemical Society 151 (9): C559-C566 2004.

D. R. Reyes, E. M. Perruccio, S. P. Becerra, L. E. Locascio, and M Gaitan, "Micropatterning neuronal cells on polyelectrolyte multilayers" Langmuir 20 (20): 8805-8811 2004.

System Design and Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution poses additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing integrated circuit (IC) contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

Metrology for System-on-a-Chip (SoC)

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M. Y. Afridi

"... the trend toward digitisation notwithstanding, the analogue content of SOCs is likely to increase."

Ron Wilson, Electronic Design News (EDN), 2006

Goals

One of the key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry is the development of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying embedded-sensor (ES) virtual-components (VCs) compatible with the System-on-a-Chip (SoC) integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC CAD libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, low-cost, smart homeland security and environmental sensor systems. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based (MicroElectroMechanical System) VCs into SoCs.

The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards, verification standards and high-level models of system components. The NIST MEMS-based integrated gas-sensing VC is used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies is used to facilitate the adoption of these MT-VCs into new Homeland Security and Industrial applications.

Customer Needs

Recent advances in high density CMOS integration and the ability to co-integrate MEMS-based sensor devices enable cost effective complex system designs fabricated on a single chip. The need for standards arises when the system-on-a-chip is designed using IP (Intellectual Property) cores from multiple vendors. These cores must be compatible for design success, thus demanding standards in the area of interoperable interfaces, models and verification strategies for multi-technology SoC designs.

The SoC design challenges include managing increasing system complexity, achieving system-level verification, and bridging the separate disciplines of system architecture and chip design. These challenges are being overcome with the use of platform-based design approaches that emphasize design reuse, *i.e.*, the development of ES-VCs that can be used as cost-effective building blocks for SoC devices, and standards for ES-VC IP interoperability with the SoC design flow.

The direct customers for this infrastructure building will be the makers of system design software, ES-SoC IP designers, SoC manufacturers and systems designers. This is generally recognized by the chip designers, manufacturers, and EDA tool developers:

"What is the most recent development that promises to truly enable a system on a chip? It is the ability to combine CMOS and MEMS structures into one process flow."

Randy Frank and Dave Zehrbach, Motorola, in *Sensors Online*, 1998

"Definitely, System-on-a-chip is the driving paradigm in our space, and there are some fundamental differences in culture and engineering mentality as well as some new technical skills that need to be developed in engineering. At the highest level, system-on-a-chip implies that you need to think like a system designer but implement like a chip designer, and those traditionally have been different disciplines..."

Shane Robison, Executive Vice President of Engineering, Cadence Design Systems, Inc. EDAcafe.com

Technical Strategy

1. To develop successfully ES-VCs for SoC design methodology, the first step in this multi-step process is to develop the ability to make the ES-VC devices via a standard CMOS compatible process. To exercise this capability we have chosen a MEMS microhotplate based embedded gas-sensor, including operational amplifiers, decoders, and an analog-to-digital converter (ADC), and a microcontroller for control and data processing.

2. The second step is to make ES-VCs compatible with the standard digital SoC design methodology. This approach will require ES-VC to incorporate digital interface circuitry and to have

the DFT/BIST (Design-For-Test/Built-In Self-Test) functionality required by SoC standards. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas-sensor VC described above.

DELIVERABLES: Develop and fabricate a fully digital gas-sensor VC in a standard CMOS 0.5-micron technology to demonstrate a standard digital interface and SoC Design-For-Test functionality. 4Q 2006

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level models (in SystemC/HDL) exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs is at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital Hardware Description Languages and higher-level system description languages such as SystemC. We are also developing methodologies to validate these models. The digital systems industry has standards set by organizations such as OCP-IP, VSIA and OSCI to foster large-scale interchange and interoperability of modular digital IP, and we believe that such standards in ES-VC field are a key factor for the growth of an ES-VC IP industry.

DELIVERABLES: Compare high-level model simulation results for microhotplate-based gas-sensor ES-VCs with measured data from a fully digital ES-VC. 3Q 2007

4. Synthesis process is well defined for the digital SoC design and is well supported by a large number of design libraries. Currently, the libraries, methodology, and standards for ES-VC synthesis do not exist. We are developing standards and metrologies for ES-VCs that will be compatible with standard digital synthesis tools.

DELIVERABLES: Develop methodology and standards to allow ES-VC to be syntheses by standard MT-synthesis tools and demonstrate their viability via our microhotplate gas-sensor VC. 2Q 2008

5. Scaling digital circuitry is a key capability used by digital designers to reduce costs and ensure compatibility with different fabrication technologies. Since most systems that would use ES-VCs will be predominantly digital, it is important that there be an equivalent scaling capability for the ES-VCs. To address the need for scaling ES-VCs, we are developing metrologies for digital-compatible scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ES-VC scaling approach and demonstrate its viability via our microhotplate gas-sensor technology. 4Q 2007

6. The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ES-VCs and interface with them via the digital shell.

DELIVERABLES: Develop methodologies for built-in self test of ES-VC devices and demonstrate their viability via our microhotplate gas-sensor technology. 3Q 2007

NIST is a natural home for this work because NIST has advanced measurement capabilities across the spectrum of sensor technologies.

Accomplishments

- A monolithic micro-gas-sensor system was successfully designed and fabricated in a standard 1.5 μm CMOS process (Fig. 1 and Fig. 2). The gas-sensor system incorporated an array of four microhotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. Digital decoders selected individual elements of the sensor array and an operational amplifier monitored sensing film conductance. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represented an improvement in sensitivity of two orders of magnitude over existing MEMS-based microhotplate gas-sensors.

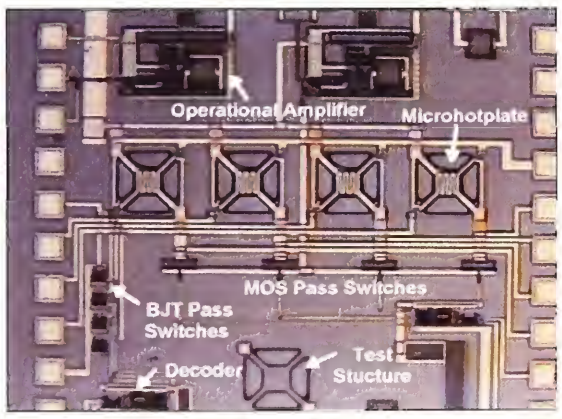

Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

- Investigated existing and emerging SoC design methodologies, and adapted digital SoC design tool-flow to enable integration of mixed-signal MEMS VCs.

- A four-element gas-sensor VC was successfully designed, fabricated and electrically characterized to demonstrate that the design approach was compatible with SoC design methodology. The performance of the 8-bit ADC exceeded the gas-sensor VC design requirements.

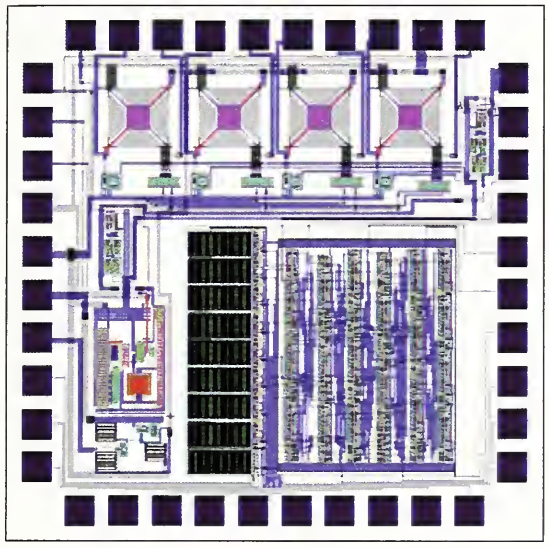

Figure 2. Layout of the four element gas-sensor VC with analog-to-digital control.

- Electrostatic discharge (ESD) protection structures were added to the gas-sensor and successfully tested (Fig. 3). These ESD test structures are based on multi-finger thyristor-type devices and are designed to achieve optimum performance and reduced area.

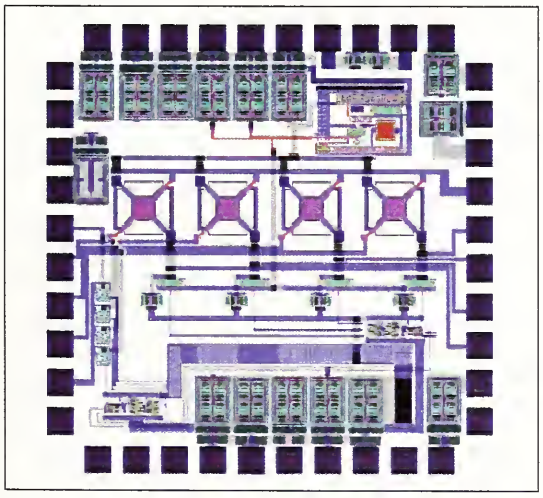

Figure 3. Layout of the four element gas-sensor VC with electrostatic discharge (EDS) protection circuitry.

- A new post-process etching technique was developed to integrate MEMS devices with standard submicron CMOS processes and a new microhotplate design that scales with standard CMOS structures and voltage levels (Fig. 4). This will enable co-integration of MEMS sensor devices with high density submicron digital systems using cost effective standard CMOS foundries. The submicron gas-sensor test chip was characterized. Characterization data showed the new scalable microhotplate will provide the temperature required for gas-sensor operation at 3.3V.

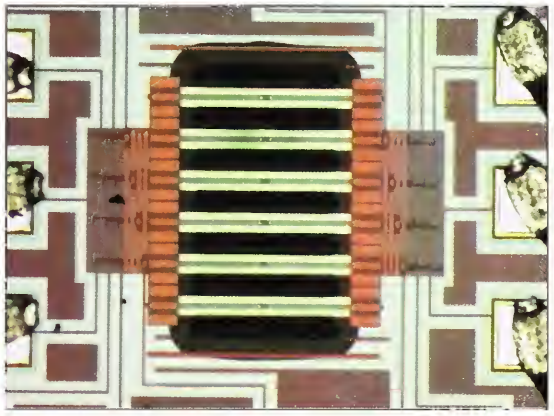

Figure 4. New microhotplate design implemented in standard submicron CMOS technology.

- Methodologies for designing digital interface shell functionality for ES-VCs were developed and demonstrated by designing the gas sensor SoC architecture.

- A high-level model of the microhotplate gas sensor ES-VC was developed. A HDL-based microcontroller core was synthesized for a 0.25 micron standard CMOS fabrication process. High-speed SystemC models of the microcontroller and microhotplate were developed to facilitate SoC software design and protocol development. This is the first time a MEMS device has been modeled in systemC and the results demonstrated the importance of including MEMS-device models in high level system modeling

- Microhotplate-based gas-sensor yield was improved by adopting a new chromium etchant.

- A computer-controlled gas-delivery system was designed, assembled, and tested. The gas delivery protocols for calibrating the microhotplate-based gas sensors were designed and implemented.

- A submicron-microhotplate test-structure chip was designed to compare the performance of

different CMOS compatible temperature sensors and to measure the contact resistance between different types of post-processed gas sensor electrodes (Fig. 5). This chip also supports the extraction of more accurate microhotplate thermal-model parameters.

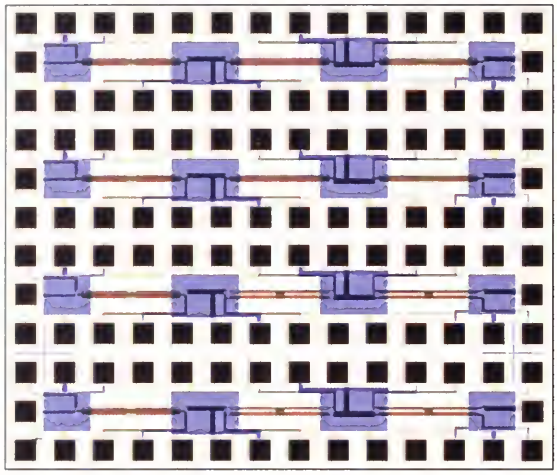

Figure 5. Layout of new microhotplate test-structure chip with different types of temperature sensors and four point electrodes for gas-sensor film contact-resistance studies.

Recognition

2005 George Abraham Outstanding Paper Award:

Y. Afridi, A. Hefner, C. Ellenwood, R. Cavicchi, and S. Semancik "Characterization System for Embedded Gas-sensor Systems-on-a-Chip" GOMACTECH 2005, pp. 94-97, 2005.

Recent Publications

J. Geist, M. Y. Afridi, A. Varma, A. R. Hefner, *"Simple Thermal-efficiency Model for CMOS-Microhotplate Design,"* J. Res. NIST (accepted 2006).

M. Afridi, A. Hefner, J. Geist, C. Ellenwood, A. Varma, B. Jacob, *"Microhotplate-Based Sensor Platform for Submicron SoC Designs,"* IEEE International Semiconductor Device Research Symposium (ISDRS), pp. 500-501, 2005.

Yaqub Afridi, Allen Hefner, Colleen Ellenwood, Richard Cavicchi, Stephen Semancik *"Characterization System for Embedded Gas-sensor Systems-on-a-Chip,"* GOMACTECH 2005, pp. 94-97, 2005.

M. Y. Afridi , A. R. Hefner Jr., D. W. Berning, C. H. Ellenwood, A. Varma, B. Jacob, S. Semancik, *"MEMS-based embedded sensor virtual components for system-on-a-chip (SoC),"* Solid State Electronics, Vol. 48, pp. 1777-1781 (24-JUN-2004).

Javier A. Salcedo, Juin J. Liou, Muhammad Y. Afridi, Allen R. Hefner, and Ankush Varma *"Electrostatic Discharge Protection for Embedded-sensor System-on-a-Chip,"* (Abs. 2587) 26th meeting of The Electrochemical Society (ECS) October 2004.

At-Speed Test of Digital Integrated Circuits

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes and developing scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit.

Customer Needs

In the device debug and characterization world, a key challenge is the development of diagnostic tools, particularly for timing information. The limitations in the current PICA/time-resolved photoemission detector technology point to the need for radically different methodologies (2005 ITRS Test and Test Equipment Section, page 9). Traditional forms of IC contact probing (fine-pitch probe cards and RF probes) technology require large contact pads incompatible with the operation and economic constraints of modern IC designs (2005 ITRS, Test and Test Equipment Section, page 24). The 2005 ITRS concludes that micro-positioner and atomic-force-microscope-based probing will be required at each roadmap generation to probe minimum sized transistors (2005 ITRS, Test and Test Equipment Section, page 9).

We are developing alternative probing approaches that use high-impedance probes, non-contact probes, and atomic-force microscopes that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. Figure 1 shows a result of the high-speed metrology we have developed, an on-chip waveform measurement to 200 GHz.

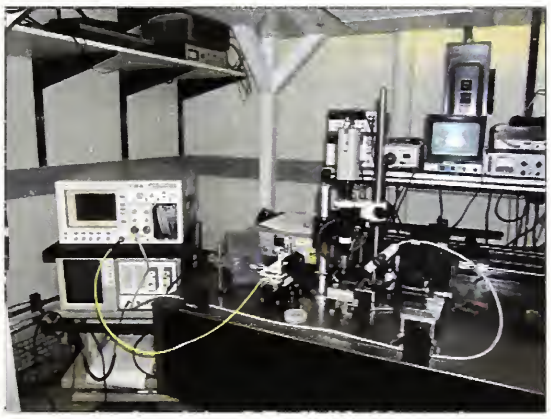

Figure 1. Three on-chip waveform measurements performed with our electro-optic sampling system.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we have constructed a universal SPM test bed for these probes. We are applying our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we plan to tie our metrology back to fully characterized electro-optic sampling measurements.

The 2005 ITRS notes that 10s or 100s of picoseconds of delay are now critical, and that there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth, and test time requirements for high performance interfaces (2005 ITRS, Test and Test Equipment Section, pages 7 and 30). To address this, we are also working on methods for calibrating and correcting imperfections in waveform measurement equipment that cause distorted or blurred measurements. These

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"As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

effects include instrument response, impedance mismatch, multiple reflections, dispersion, timebase distortion, jitter, and drift. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system. Our calibration strategy is independent of the particular signals being measured and is applicable to digital, RF/microwave, and mixed signal systems, enabling the single platform measurement solutions called for in the 2005 ITRS, Test and Test Equipment Section, page 36.

DELIVERABLES:

- Fabricate and verify functionality to 50 GHz of generator circuits based on photoconductive switches suitable for the construction of portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales. 2Q 2006
- Optimize the response of the fiber optic field probe by design and control of the reflectivity of the integrated MEMS mirrors. 3Q 2006
- Demonstrate the capability to measure the thermal fluctuations of a single cantilever with the integrated probe. 4Q 2006
- Demonstrate the capability to measure time-domain insertion delay of a coaxial cable with 1 ps resolution. 4Q 2006

Accomplishments

- We have designed and tested a prototype sinusoidal waveform standard.
- We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power.
- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.
- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.
- We have constructed an SPM universal test bed.
- We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.
- We have developed a procedure for testing high-impedance probes directly on our electrooptic sampling system. This system has a calibrated bandwidth of 200 GHz.
- We have demonstrated a method for correcting oscilloscope timebase jitter, drift, and distortion.
- We have fabricated fast photoconductive switches and demonstrated a rise time of better than 5 ps, largely exceeding our goal of constructing generator chips useable to 50 GHz. We will use these to construct a portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales (see Fig. 2).

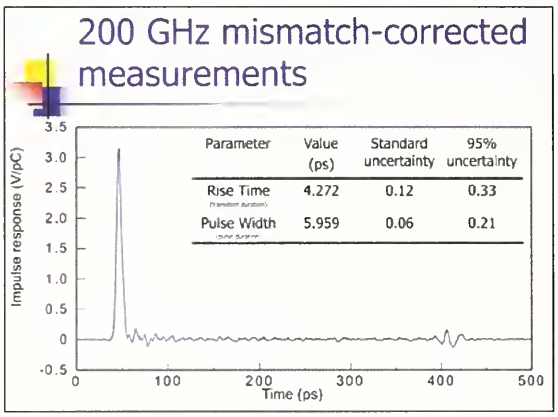

Figure 2. Measurement system used to verify the functionality of our photoconductive switches.

- We developed the fabrication process for creating the MEMS chips with integrated 45-degree mirrors and trenches for fiber alignment (see Fig. 3).

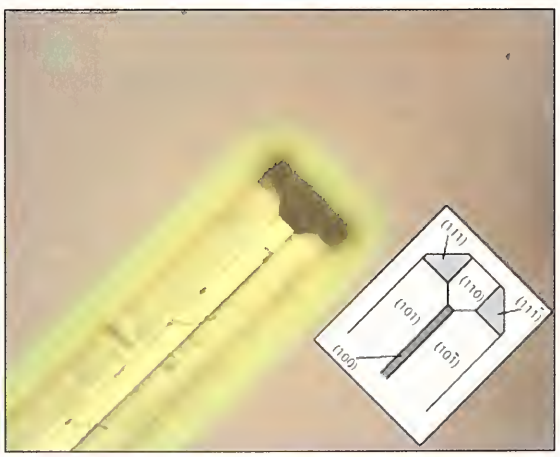

Figure 3. The Fiber-optic trench with integrated 45-degree mirror.

- We assembled the fiber optic interferometer for the measurement of the deflection of the cantilevers including the thermal feedback control.

Recent Publications

T. S. Clement, P. D. Hale, D. F. Williams, C. M. Wang, A. Dienstfrey, and D. A. Keenan, *"Calibration of sampling oscilloscopes with high-speed diodes,"* accepted for publication in IEEE Trans. Microwave Theory and Tech., 2006.

A. Dienstfrey, P. D. Hale, D. A. Keenan, T. S. Clement, and D. F. Williams, *"Minimum-phase calibration of sampling oscilloscopes,"* accepted for publication in IEEE Trans. Microwave Theory and Tech., 2006.

D. F. Williams, A. Lewandowski, T. S. Clement, C. M. Wang, P. D. Hale, J. M. Morgan, D. A. Keenan, and A. Dienstfrey, *"Covariance-based uncertainty analysis of the NIST electro-optic sampling system,"* IEEE Trans. Microwave Theory and Tech., Jan. 2006.

D. F. Williams, H. Khenissi, F. Ndagijimana, K. A. Remley, J. P. Dunsmore, P. D. Hale, C. M. Wang, and T. S. Clement, *"Sampling-Oscilloscope Measurement of a Microwave Mixer with Single-Digit Phase Accuracy,"* accepted for publication in IEEE Trans. Microwave Theory Tech.

P. D. Hale, C. M. Wang, D. F. Williams, K. A. Remley, and J. Wepman, *"Compensation of random and systematic timing errors in sampling oscilloscopes,"* accepted for publication in IEEE Trans. Instrum. Meas., 2006.

S. Lee, Y. C. Lee, T. M. Wallis, J. Moreland, and P. Kabos, *"Near field imaging of high-frequency fields with calorimetric cantilever probes,"* Journal of Applied Physics, 99, pp. 08H306-1-08H306-3, (2006).

D. F. Williams, P. D. Hale, T. S. Clement, and J. M. Morgan, *"Calibrated 200 GHz Waveform Measurement,"* IEEE Trans. Microwave Theory and Tech., April, 2005.

T. M. Wallis, J. Moreland, W. Riddle, and P. Kabos, *"Microwave power imaging with ferromagnetic calorimeter probes on bimaterial cantilevers,"* Journ. of Mag. and Magn. Mater, vol 286, pp. 320-323 (2005).

Thermal Measurements and Packaging Reliability

Goals

Our goal is to provide the microelectronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens that present a reliability concern to the manufacturer or end-user, or a model system is fabricated in-house. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal — providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allow us to refine the techniques to make them optimally beneficial to industry, and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, which is essential for technology transfer.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (*e.g.*, SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs) and enables the measurement of transient current constriction failure events in RF and high power devices. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for *in-situ* measurement of heat transfer performance degradation after various levels of thermal stress such as power cycling, thermal cycling and thermal shock.

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging and interconnects are many and display a variety of thermal responses that are not always compatible. This makes interconnect lines and interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: (1) predicting reliability or operating life of device, (2) measuring material/device thermal properties *in-situ*, (3) confirming or determining the operating limits or thermal performance of a device, and (4) validating thermal models for device, chip and system performance. Thermal measurements on small, <10 μm structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to "Moore's Law." Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing

Technical Contacts:
A. J. Slifka
A. R. Hefner

"I am writing to let you know that NIST has been of great assistance to Cenymer Corporation, one of our portfolio companies. This portfolio company has developed a novel material. Dr. Andrew Slifka at NIST was able to provide the company with thermal measurements that are critically important to Cenymer as it approaches potential customers. It is great to have NIST in the community as a resource to companies like Cenymer."

Tim Connor
Sequel Venture Partners

the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs. System level power reduction strategies are generally recognized by the ITRS 2005 as necessary for the continual advancement of electronic systems at a rate consistent with "Moore's law."

"As the thermal resistances are made smaller and smaller for high power devices, thermal metrology with better resolution and capabilities is required. For example there is strong need to establish industry wide transient thermal measurement technique standard." ITRS 2005.

"Power consumption is now the major technical problem facing the semiconductor industry. As feature sizes shrink below 0.1 micron, static power is posing new low-power design challenges. ITRS predicts a decrease in dynamic power per device over time. However, the doubling of on-chip devices every two years would force an increase of current leakage on a per-chip basis." ITRS 2005.

"New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key." 2005 ITRS: one of the five "Difficult Interconnect Challenges"

"As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion." 2005 ITRS: one of the five "Difficult Interconnect Challenges"

Technical Strategy

1. We are developing techniques in scanning thermal microscopy, utilizing the AFM (atomic force microscope), which have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What is the interfacial thermal resistance of an alloy/intermetallic interface." The first was answered using the IR microscope; the second has yet to be answered. Determining temperature and temperature distribution at the micron and submicron size scales and additionally in the time domain will aid in determination of failure mechanisms in packages and interconnects.

We have just completed our fourth year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability, and have engendered great interest from the Advanced Embedded Passive Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute increase in interfacial thermal conductivity is the first indication of the microcracks and fissures that ultimately may result in failure.

DELIVERABLES: Scanning Probe Microscope (SPM) calibration devices for thermal SPM designed and fabricated. 2Q 2006

2. As the size of packages gets smaller, heat removal becomes a more significant problem. The SPM is being used to develop a technique to measure thermal conductivity of thin films for application to metal interconnect lines. The technique also will be able to measure interfacial thermal resistance between coatings and substrates. The theoretical work on this development is being done in collaboration with Dr. Kevin Cole of the University of Nebraska.

DELIVERABLES: Refine the theory in conjunction with development of increased measurement accuracy. 3Q 2006

3. Carbon nanotubes have potential in heat-removal applications and in wear applications. Thermal properties show great promise in this area, if production issues can be addressed. We are currently measuring carbon nanotubes made from different inexpensive processes to determine if heat removal applications are economically and technologically feasible.

DELIVERABLES: Measure interfacial thermal resistance of carbon nanotube-covered copper and baseline copper materials. 2Q 2006

4. Thermomechanical fatigue of interconnect lines is an important reliability issue as lines become smaller. Using thermal scanned-probe microscopy, we are measuring temperatures of damaged locations on lines and temperature distribution on and around interconnect lines to elucidate failure mechanisms and predict lifetimes.

DELIVERABLES: Measure lines both temporally and spatially. Report results in literature. 4Q 2006

5. High speed temperature sensitive parameter (TSP) measurements are required for in-situ evaluation of the heat transport through the interface of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and DBC isolation attach degradation after thermal cycling and thermal shock stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design.

DELIVERABLES: Perform thermal cycling and thermal shock stress on DARPA Wide-Bandgap High Power Electronics program devices and American Competitiveness Institute ManTech devices. Use unique NIST high speed, high current TSP system to evaluate die attach and DBC attach integrity before and after thermal stress. 4Q 2006

6. A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high speed transient measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1-μs temporal resolution and 15 μm spatial resolution. The new system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions and enables the measurement of transient heating events such as reduced power IC FUBs (clock gating, dynamic voltage scaling, and Vdd gating), enables the measurement of transient current constriction failure events in RF and high power devices, and measurement of current uniformity in large area power devices.

DELIVERABLES: Apply high speed thermal imaging system to characterize localized dynamic heating of reduced power FUBs in advanced digital integrated circuits. 4Q 2006

DELIVERABLES: Improve the spatial resolution of the NIST high speed transient thermal imaging system from 15 μm to 3 μm while maintaining the 1-μs time resolution. 4Q 2007

7. There is a strong need to establish industry wide transient thermal measurement technique standards as described in the 2005 ITRS roadmap. NIST recently developed and tested a transient thermal calibration test structure with 1-μs temporal resolution using micro hotplates with integrated temperature sensors. The set of calibration test structures is now being expanded to develop a prototype IR transient thermal imaging calibration test chip.

DELIVERABLES: Complete development of prototype IR transient thermal imaging calibration test chip. 3Q 2007

Accomplishments

- Since there is no commercially available device for calibration of a thermal atomic-force microscope (AFM) probe tip, we developed 6 different designs and evaluated the electrical performance as a function of temperature. We also chose the best design for use with the AFM in both steady-state and transient thermal modes. Figure 1 shows the device.

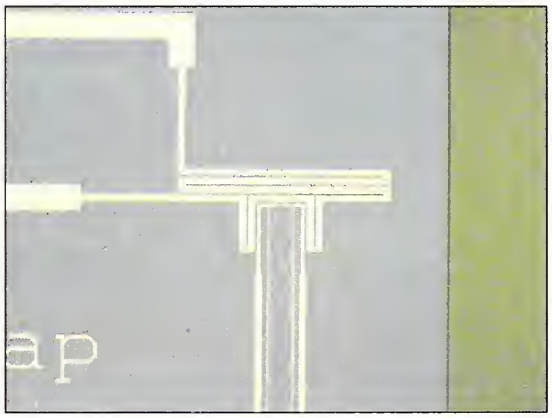

Figure 1. A microdevice with an integral heater and sensor for calibration of thermal probe tips.

- The change in resistance as a function of temperature of the sensor will be used to calibrate AFM probe tips. Figure 2 (page 208) shows the calibration curve for one of the devices.

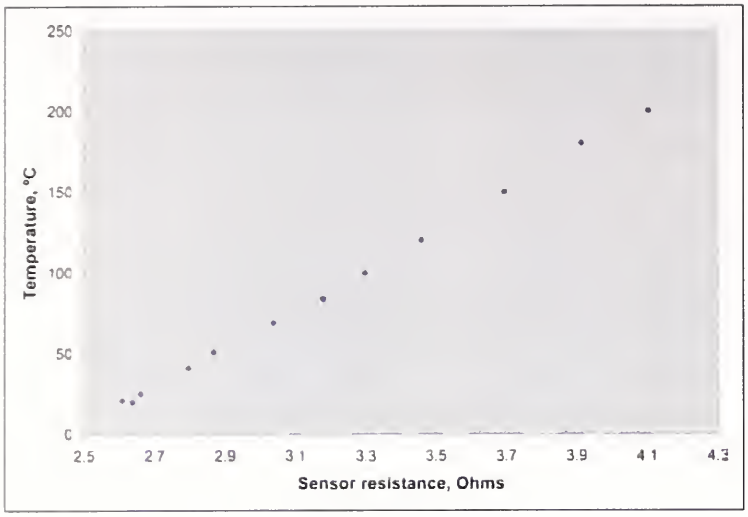

Figure 2. Calibration curve from a NIST microdevice showing device temperature as a function of sensor resistance.

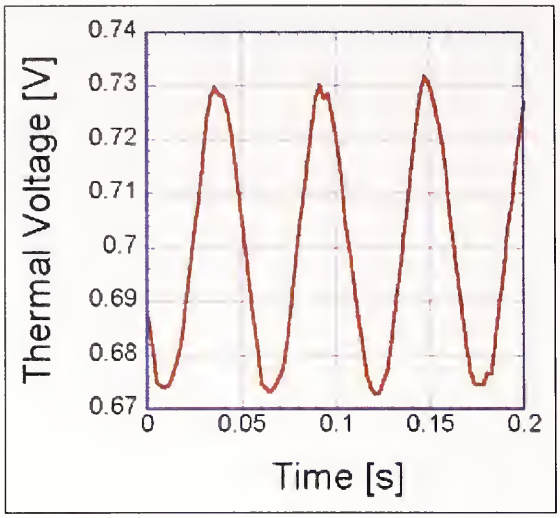

Figure 3. Sample data showing time-resolved thermal fluctuations of an interconnect line during A.C. heating.

■ Feasibility has been shown of measurements of electronic interconnect lines using the thermal SPM. We are now calibrating the response of the probe tip to temperature.

■ The measurement of thermomechanical fatigue is done in a transient fashion at a rate on the order of 100 Hz. The electronics that control the thermal scanned-probe microscope have specifications from the manufacturer that state that the thermal settling time constant is 350 microseconds due to the thermal mass of the probe tip. Therefore, transient measurements up to 2800 Hz should be possible. To determine feasibility of measuring thermomechanical fatigue, we have made measurements using the thermal probe tip on an interconnect line that was being heated at 100 Hz a.c. Figure 3 shows a plot of data from the thermal microscope in the form of thermal voltage as a function of time. A calibrated probe tip will allow us to present this data in the form of temperature as a function of time. Two papers were written that include some results, R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, "Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects," submitted to *Metallurgical and Materials Transactions* April 2006, Paper presented at the 2006 TMS Annual Meeting, and R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, "Electrical Methods for Mechanical Characterization of Interconnect Thin Films," 2005 Advanced Metallization Conference.

■ We have been making measurements of carbon nanotube mats grown on copper substrates as a potential replacement for copper-and-thermal-grease heat sinks. Measurements of two copper specimens with thermal grease between all three interfaces was compared with two carbon nanotube (CNT) specimens placed face-to-face, with thermal grease between the measurement plates and copper blank sides at low contact pressure (finger-tight, 555 psi). Figure 4 shows the results. Even at this low contaet pressure, before the CNTs begin developing large amounts of tube-to-tube contact, the CNT specimens outperform the copper with thermal grease.

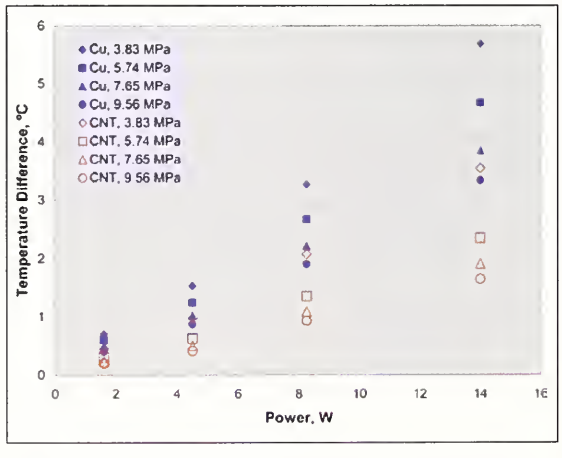

Figure 4. Comparison of temperature differences across thermal-grease-and-copper interfaces and carbon nanotubes.

■ Development of the high-speed (1 μs) transient thermal imaging system was completed. The acquisition and data analysis capabilities of this system have been extended to include a burst method and to allow frames from different transient movies to be compared more readily. An auto-scaling capability and user definable number of frames have also been added. A thin carbon-black chip coating process was developed to improve sample emissivity without altering the chip surface thermal response time.

■ NIST recently developed and tested a transient thermal calibration test structure with 1 μs temporal resolution using micro hotplates with integrated temperature sensors. This specially designed temperature-reference microhotplate structure is calibrated and used to verify the results of the transient IR thermal imaging system. Figure 5 compares the single point IR transient response with the electrically measured transient response of a microhotplate structure for a 20 μs heating pulse.

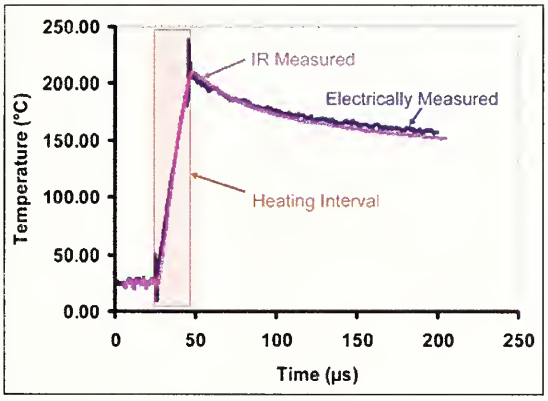

Figure 5. Microhotplate thermal response to a 20 μs heating pulse (as indicated) measured with both IR and electrical methods.

■ As low-degradation rate SiC PiN diodes are beginning to emerge, the NIST transient thermal imaging system is being used to determine the current uniformity after various levels of stress up to 1000 hours of operation. The pulsed thermal image results show that the current is relatively uniform before degradation and that only 1 % of the chip is conducting all of the current after substantial degradation. Degradation of SiC diodes remains highly variable, as demonstrated in Figs. 6a and 6b. Figures 6a and 6b are current uniformity images of two different SiC 10 kV, 20 A diodes operated at full rated current for 500 hours under forward bias. The diode shown in Fig. 6a shows good current uniformity after 500 hours operation and the diode shown in Fig. 6b demonstrates highly non-uniform current conduction after 500 hours operation as represented by the non-uniform high-speed pulsed temperature map (only 50 % of device is conducting).

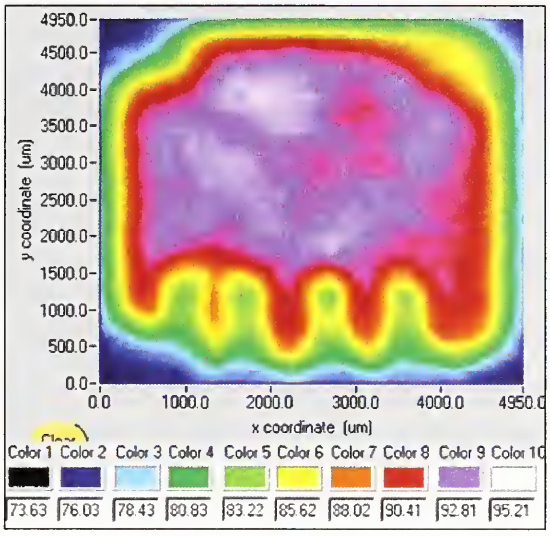

Figure 6a. SiC diode relative temperature uniformity map shows relatively uniform current conduction throughout the chip after 500 hours stress at full current. The four green areas at the lower part of the chip are caused by wire bond shadowing of the thermal radiation.

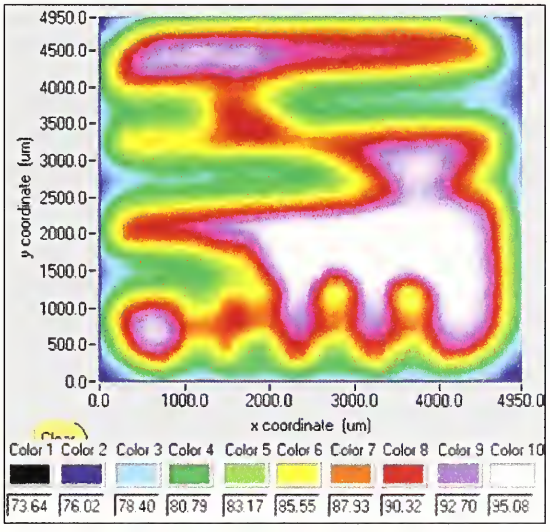

Figure 6b. Relative temperature uniformity map for a similar SiC diode shows highly non uniform current conduction after 500 hours stress at full current. Both of these diodes are mounted on a temperature-controlled heatsink and the background temperature is 75 °C.

- NIST has developed a method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS}, at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter (TSP). This TSP method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module).

- The high-speed TSP method was applied to compare the heating response measurement with the thermal model for a commercial high power IGBT half bridge module, commercial six-pack IGBT module, and prototype NSF Center for Power Electronic Systems Module. Electro-thermal simulations of a full three-phase inverter have been successfully performed and compared with measured results of the power converter temperature monitors.

- The hardware construction and computer interfacing for the NIST high power rapid thermal cycling/shock test system were completed. This included necessary electronics instruments, flow controllers, high thermal impedance plumbing interfaces, and computer control of air flow rate, water flow rate, and heater power PID temperature controller. The system produces 300 °C thermal cycles with computer programmable temperature rise and fall times.

Collaborations

University of Nebraska: Kevin Cole

Cenymer Corporation: Scott Joray

Cynthia Volkert, Forschungszentrum Karlsruhe, Germany

Reiner Mönig, MIT, Cambridge, MA

Glenn Alers, Novellus Inc.

Michael Lane, IBM, Yorktown Heights, NY

Ju-Young Kim, Seoul National University, Korea

Roop Mahajan, University of Colorado

Amit Khosla, Motorola

Krishna Ramadurai, University of Colorado

University of Puerto Rico Mayagüez: Miguel Velez

University of Maryland: Bruce Jacob

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

American Competitiveness Institute (ACI), Navy ManTech center: Barry Thaler

Recent Publications

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* submitted to Metallurgical and Materials Transactions, Paper presented at the 2006 TMS Annual Meeting (April 2006).

R. R. Keller, C. A. Volkert, R. H. Geiss, A. J. Slifka, D. T. Read, N. Barbosa III, and R. Mönig, *"Electrical Methods for Mechanical Characterization of Interconnect Thin Films,"* 2005 Advanced Metallization Conference.

J. R. Reichl, J.-S. Lai, A. R. Hefner, T. R. McNutt, D. Berning, D., *"Inverter Dynamic Electro-Thermal Modeling and Simulation with Experimental Verification,"* IEEE Power Electronics Specialists Conference, pp. 2208-2215 (June 2005).

A. R. Hefner, T. R. McNutt, A. Akuffo, R. Singh, C. Ellenwood, D. Berning, M.K. Das, J. J. Sumakeris, and R. Stahlbush, *"Characterization of SiC PiN Diode Forward Bias Degradation,"* Volume: 2 , pp.1252-1260 (Oct. 2004).

Blackburn, D. L., *"Temperature Measurement of Semiconductor Devices – A Review,"* Proceedings of Semiconductor Thermal Measurement and Management Symposium, pp. 70-80 (March 2004).

J. Reichl, D. Berning, A. Hefner, and J-S. Lai, "Six-Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation," *IEEE Applied Power Electronics Conference*, Anaheim, CA (Feb. 2004).

Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data.

Factory Time Synchronization Standards Development for E-Manufacturing

Technical Contact:
Y. Li

Goals

The project's objective is to facilitate the development of standards and guidelines to achieve reliable clock synchronization and time stamping capabilities for supporting present and future e-Manufacturing needs. The project aims to educate the industry about the requirements, related issues, and potential solutions in regards to distributed precision clock synchronization.

Customer Needs

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the ehallenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Advancing next-generation semiconductor manufacturing will require data to be collected and analyzed from a rising confluence of data streams, due to narrowing tolerance windows, new material introduction and novel processing techniques. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

One of the projected near term Factory Integration difficult challenges in the International Technology Roadmap for Semiconductors (ITRS) is managing the increasing factory complexity which results in:

"Explosive growth of data collection/analysis requirements driven by process and modeling needs..." 2005 ITRS Edition, Factory Integration, p. 3.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data. Accurate time stamps will become a key component in data quality for Advanced Process Control (APC) applications, especially in the realm of Fault Detection Classification (FDC). Quality time stamps ensure the ability to precisely pin-point cause-effect relationships.

"A prerequisite to APC deployment is thus acceptable levels of data quality provided by the tool, metrology, and sensors. Data quality issues include availability, timeliness (of data capture and delivery), accuracy, resolution, freshness, and contextual richness (including time stamping)." 2005 ITRS Edition, Metrology, p. 38.

With the advent of the Equipment Data Acquisition (EDA) interface where data collection rates can increase to 10,000 data points per second, one millisecond time stamp accuracy will be required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

Technical Strategy

Through active participation in the SEMI Time Synchronization Working Group, this project will continue to investigate and document key industry requirements and work with industry and academia to develop effective guidelines and standards to facilitate deployment of distributed clock synchronization and accurate time stamping.

The first approach is to improve understanding of the latest developments in evolving distributed clock synchronization technologies, specifically in the mainstream protocols such as IEEE 1588, *Precision Clock Synchronization Protocol for Networked Measurement and Control Systems,* and NTP, *Network Time Protocol.* The semiconductor industry requirements have been presented to the IEEE 1588 group in order to leverage feedback on recommended practices.

DELIVERABLES: Document semiconductor industry precision clock synchronization requirements for the IEEE 1588 committee. 1Q 2006

To expedite integration of time synchronization protocols into the equipment, standards will be necessary to make the tasks as efficient as possible. The SEMI Time Synchronization Working Group has also completed discussions in a summary of industry requirements in order to provide equipment suppliers and chip manufacturers with guidance of upcoming needs. Equipment suppliers would like to understand the key application needs in order to prioritize the design of their next-generation tools to fit industry timing requirements. A review of current SEMI standards is also needed to mitigate conflicts with the upcoming time synchronization standard and gaps between current standards and new requirements.

DELIVERABLES: Review of current SEMI Information and Control Standards and document gaps with current requirements and potential conflicts with upcoming time synchronization standard. 2Q 2006

To enable accurate time stamping, it is imperative to have a reliable and accurate clock synchronization methodology. Research on practical application and performance testing of the synchronization protocols would determine the impact of various computing factors (*e.g.*, CPU usage, network traffic, etc.) on distributed clock synchronization performance. The Engineering Research Center at University of Michigan has been collaborating with NIST in conducting studies on the accuracies achievable with software-based time synchronization protocols in industrial networks. The work will have practical benefits in ensuring the potential solutions and new industry standards are feasible and effective in achieving accurate clock synchronization and data time stamping.

DELIVERABLES: Conduct research and document methodology, results and recommended practices on the impact of network node delays on IEEE 1588 precision clock synchronization performance. 4Q 2006

Accomplishments

- A NIST internal report (NISTIR 7184) on "Semiconductor Factory and equipment Clock Synchronization for e-Manufacturing" was published in December 2004.

- The presentation on *"Running Out of Time:* Improvements Required in Current Semiconductor and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection" was given at AEC/APC Symposium in September 2004.

- *"Intricacies of Time:* Demystifying Clock Synchronization and Time Stamping for e-Manufacturing" was presented at AEC/APC Symposium in September 2005.

- *"In Search of the Key to the Lock:* Clock Synchronization Requirements in Semiconductor Manufacturing" was presented at the IEEE 1588 Conference in October 2005.

- "Using Network Time Protocol (NTP): Introduction and Recommended Practices" was published as an ISMI Technical Report in February 2006.

- "Legacy Standards Update: SEMI Standards Analysis to Meet Factory Time Synchronization Requirements" was presented at the SEMI Spring IEE TF meeting in March 2006.

- Poster presentation on "New Industry Requirements for Clock Synchronization and Time Stamping" was published at the European AEC/APC Symposium in March 2006.

- "Time Synchronization in Manufacturing Networks" at the Network Performance Workshop (University of Michigan) was presented in April 2006.

Collaborations

Harvey Wohlwend, Gino Crispieri, International SEMATECH Manufacturing Initiative

James Moyne, Engineering Research Center, University of Michigan Ann Arbor

Alan Weber, Alan Weber and Associates

E-Diagnostics Security

Technical Contacts:
Y. Li
K. Brady

Goals

The project strives to employ the latest web services security technologies for mitigating increasing security risks of potential Internet-based application systems, such as e-Diagnostics. As a proof of concept, the project aims to design a web-based framework that leverages available security technologies to ensure proprietary semiconductor process and equipment data would not be compromised.

Customer Needs

E-Diagnostics enables equipment suppliers to remotely monitor, maintain, diagnose, and repair tools on the factory floor. Enabling a web-based application would provide greater flexibility for equipment engineers to monitor or troubleshoot equipment on the manufacturing floor. With the convenience and economic advantages of being able to diagnose and resolve problems via the Internet come all the security challenges of the digital world. The challenges in managing Internet-based security have been a critical obstacle in using web services for e-Diagnostics. However, the web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. A web services security framework would provide an initial step towards realizing a web-based e-diagnostics system. A framework infrastructure promotes interoperability and rapid integration of new security technologies to ease the management of dynamic security policies with the proliferation. As cyber-based attacks become increasingly sophisticated, defenses must evolve to ensure intellectual property remain protected, and factory systems would be able to defend against attacks and have the mechanisms to rapidly detect and isolate security attacks. Security in factory integration systems has become one of the latest key focus areas for International Technology Roadmap for Semiconductors (ITRS):

"Cyber infections such as viruses, worms and denial of services have made security a key focus area with the potential of disrupting factory operations due to downtime and reduced manufacturing productivity." 2005 ITRS, Factory Integration, p. 17.

In addition to threats of viruses and worms, robust authentication and access control of legitimate users must be in place. The system should be readily managed to accommodate dynamic security policies. Simplifying security management is a key practice in avoiding security loopholes. Therefore, in facing the proliferation of security threats and system vulnerabilities, the industry can benefit by leveraging mainstream security tools to provide a robust line of defense against potentially costly threats to intellectual property and the continuous operation of factory systems.

Technical Strategy

The web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. The extensible Markup Language (XML) security suite provides a standard paradigm to manage access control in order to restrict who may and may not control the equipment remotely, encryption and signatures in order to protect the data and ensure against malicious attackers, and key management to ensure the encryption used is safe. These features work with web services transport systems such as Simple Object Access Protocol (SOAP) to further ensure the safety of the data passed in transit. Leveraging the available standards in an effective manner can serve as a potential line of defense. However, employing XML-based standards alone are not sufficient in implementing a secure framework. Security must be managed through careful interaction with factory systems, databases and networks, as well as the users accessing the factory systems. With a plethora of choices available in implementing web-based security, it is imperative to select the key security concepts necessary to enable a robust yet simple web-based security infrastructure for the e-diagnostic environment.

DELIVERABLES: Research and document key web services security technologies to enable a web services security framework and recommended practices. 3Q 2006

Based on the needs of industry, a framework will be designed and implemented that allows for fine-grain access control to restrict unauthorized users from infiltrating the system, while ensuring legitimate users have convenient access to resources necessary to complete their tasks. The framework will include a method for logging each transaction to enable auditing of all those who accessed the system and track which actions were performed while a user was logged

in. Additional information would also be readily extracted from the logs to establish a workflow for tracking equipment maintenance status via the Internet. In order to strengthen the system, we will incorporate the current web-services security technologies available to encrypt messages and secure transportation of all sensitive information. The result of the project would be a prototype to demonstrate a secure web services framework for e-Diagnostics and other web-based applications in the semiconductor industry.

DELIVERABLES: Design, implement and evaluate a web-based security framework and document results and recommended practices in using security technologies for web-based e-Diagnostic applications. 4Q 2006

Accomplishments

- Draft white paper on "Survey of Web Services Security Technologies and Recommended Practices."

- Initial software undergoing development by NIST and ESIAL is available at: http://e-diagnostics.sourceforge.net/.

Collaborations

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Engineering Chain Management in the Semiconductor Industry

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Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry's hopes to reduce time, inventory, and therefore costs.

"It is expected that improvements in manufacturing productivity will play an even greater future role in reducing time to money and getting the most out of factory investment." 2004 International Technology Roadmap for Semiconductors Factory Integration (ITRS) Overview Update, p.52.

The transition to 300 mm fabs and single-wafer lots has challenged the semiconductor industry in nearly every aspect of production, such as: facility layout; the mix of R&D within a single fab; data analysis of small lots; tool to tool interconnect; automated material handling and tracking of product, non-product wafers and reticles; the division of the production process across a partnership of foundries, designers, production sites, distributors and equipment manufacturers. Chip manufacturers require greater visibility of end product demand to accurately schedule their factories, and require greater technical collaboration with designers, OEMs, and foundries to ensure the manufacturability of the product being designed today using the generation of equipment that will be installed once production starts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2003 ITRS, p. 1.

According to the 2003 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. Intellectual Property (IP) reuse helps companies get complex systems to market quickly by eliminating redundant design effort. Standard formats for IP specifications and tool interfaces for the design of a System-on-a-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

An additional factor affecting design is the growing trend towards environmental legislation that seeks to protect the environment from hazardous substances. An example of this new trend is the European Union's Restriction of Hazardous Substances (RoHS) in electronics directive that seeks to reduce or eliminate six substances known to be hazardous to humans and the environment. This will result in a massive shift in the availability of parts as some components are removed from the marketplace while others are redesigned completely to remove the banned substances. In addition to forcing product changes, the only way for companies to comply with such legislation will be to support the exchange of material composition information throughout the entire supply chain. Complying with the new legislations will greatly add to the cost of design and can only be mitigated through the development of appropriate standards.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Chair the Product Lifecycle Information Management (PLIM) TWG of the ITRS 2006 Roadmapping Activity. 4Q 2006

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: Establish a working arrangement with ISMT and SEMI in order to identify top industry IT-standards related needs and develop potential solutions to the current challenges based on cross-industry solutions facing similar issues. 3Q 2006

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Working with industry create a material declaration standard to assist industry with complying with the RoHS directive. 2Q 2006

Accomplishments

- Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

- NIST has been co-leading the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Initial efforts are being made to determine the scope and identify the challenges of creating an effective Engineering Chain.

- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

SEMATECH

NIST/SEMATECH E-Handbook of Statistical Methods

Goals

The goal of the *NIST/SEMATECH e-Handbook of Statistical Methods* project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the *e-Handbook* readily accessible to its target audiences in industry, including the semiconductor industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH (Fig. 1).

DELIVERABLES: Update and maintain the *e-Handbook* on-line, and continue to distribute the *e-Handbook* on CD for off-line use. 4Q 2006

Accomplishments

Since release of the final version, work has focused on publicizing the *e-Handbook*, responding to user feedback, and developing a compact disk version for off-line use (Fig. 2). The web version of the e-Handbook averages approximately 1 million hits per month and over 8,000 e-Handbook compact disks have been distributed to industrial, government, and academic users all over the world over the last two years. Publicity on the e-Handbook has appeared in *Science, Quality Digest, MicroMagazine.com, States News Service, National Science Digital Library Report for Math, Engineering, and Technology*, and *American Statistician*.

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

Figure 1. NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

Recent Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.

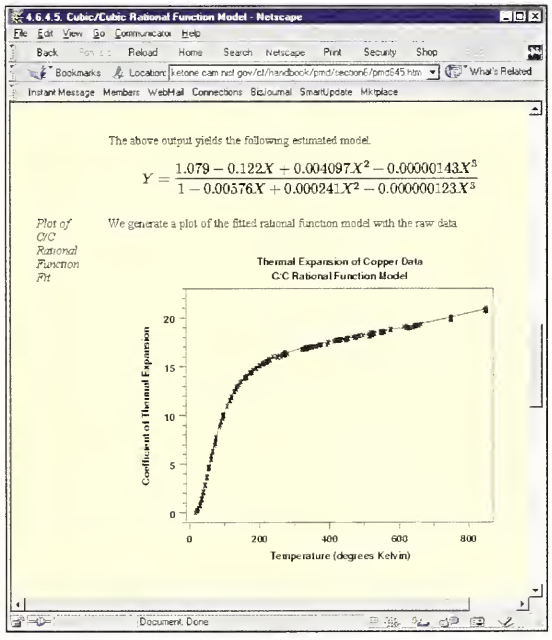
4.6.4.5. Cubic/Cubic Rational Function Model - Netscape
The above output yields the following estimated model.
$$Y = \frac{1.079 - 0.122X + 0.004097X^2 - 0.0000143X^3}{1 - 0.00576X + 0.000241X^2 - 0.000000123X^3}$$
Plot of C/C Rational Function Fit
We generate a plot of the fitted rational function model with the raw data
Thermal Expansion of Copper Data
C/C Rational Function Model
Coefficient of Thermal Expansion
Temperature (degrees Kelvin)
Document: Done

Figure 2. Page from a case study in the process modeling chapter of the Handbook.

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"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc.

Abbreviations and Acronyms

A.C.	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CPU	Central Processing Unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
D.C.	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing

DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal Oxidation Of Silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	MicroProcessor Unit
MUX	multiplex

NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown

TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
XRR	X-Ray Reflectometry

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